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Abstract

In this paper, the effects of process variations in a HCMOS (High-Speed Complementary Metal Oxide Semiconductor) IC (Integrated Circuit) are examined using a Monte Carlo SPICE (Simulation Program with Integrated Circuit Emphasis) simulation. The variations of the IC are L and VTO variations. An evaluation method is used to evaluate the effects of the variations by modeling it using a normal (Gaussian) distribution. The simulation results show that the IC may be detected as a defective IC caused by the variations based on large supply currents flow to it.

Keywords: *Process Variations, High-Speed Complementary Metal Oxide Semiconductor Integrated Circuit, Monte Carlo, Normal Distribution*

1. Introduction

A HCMOS (High-Speed Complementary Metal Oxide Semiconductor) IC (Integrated Circuit) is a family of CMOS (Complementary Metal Oxide Semiconductor) ICs [1]. Thus, it consists of p-type and n-type MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) [2]. However, it has lower power dissipation than that of the CMOS ICs.

A CMOS IC is identified by six masks, i.e., n-well, polysilicon, n+ diffusion, p+ diffusion, contacts, and metal. There are many processes required to fabricate the CMOS IC by creating the masks, such as lithography, dopant, and others [3]. Each process may generate variations during IC fabrication caused by operating conditions [4]. Unfortunately, the process variations may affect performances of the IC [5].

Process variations of the IC are channel length L, threshold voltage VTO, and oxide thickness TOX variations [6]. However, the TOX variation causes minor effects compared to others [7]. Thus, the effects of the L and the VTO variations should be evaluated.

The L variation may be triggered by lithography limitation [8]. On the other hand, the number of dopant atoms may cause the VTO variation [9]. Both of the L and the VTO variations may cause the IC experiences error in its operation [10].

A faulty CMOS IC was detected by an IDDQ testing [11]. The faulty might be caused by an open defect of a metal in an input gate. The testing was based on measuring a quiescent supply current IDDQ of the IC. The testing shows that the large quiescent supply current IDDQ will flow to the IC when the open defect is detected. By using this phenomenon, an IC is detected as a faulty by flowing a large quiescent supply current IDDQ to it.

In this paper, a Monte Carlo SPICE (Simulation Program with Integrated Circuit Emphasis) simulation is proposed to evaluate the effects of L and VTO variations in a HCMOS IC. The variations are modeled by a normal (Gaussian) distribution; afterwards, they are examined using the SPICE simulation of LTSpiceIV. The simulation results are then compared to the faulty IC [11]. A HCMOS IC may be detected as a defective IC caused by L and VTO variations based on large quiescent supply currents IDDQ flow to it.

2. Evaluation Method

In order to evaluate the effects of L and the VTO variations of a HCMOS IC, the variations are modeled by a normal (Gaussian) distribution [12]. The distribution is depicted in Figure 1. As shown in Figure 1, μ and σ are a mean and a standard deviation respectively.

A HCMOS IC design in Figure 2, *IC#i*, is made to evaluate the effects of the variations. The design consists of input protection circuits, input inverters, a logic core, output inverters, and output protection circuits.

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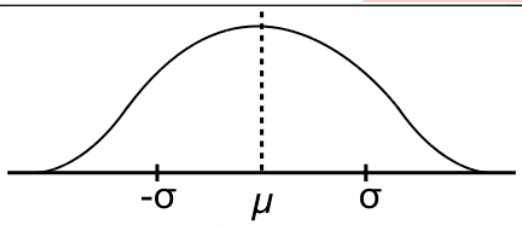


Figure 1. Gaussian Distribution

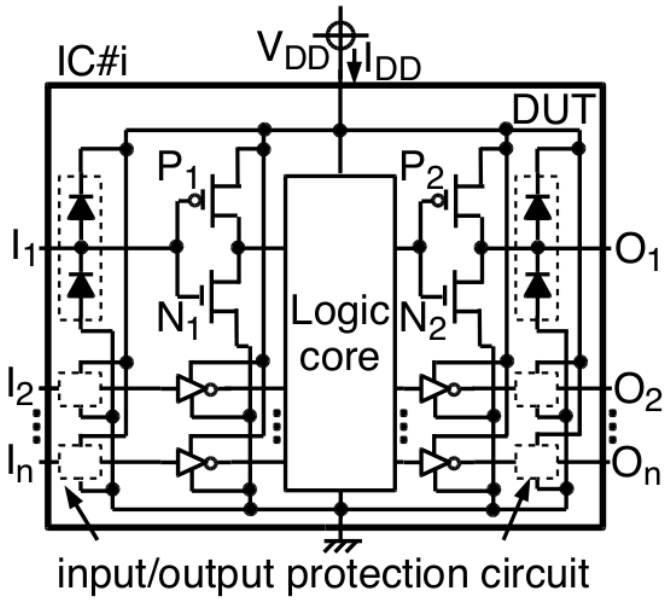


Figure 2. Design of Evaluation IC

As shown in Figure 2, a supply voltage V_{DD}, a supply current I_{DD}, input pins I_1 to I_2, and output pins O_1 to O_n are provided to the design. The core may be inserted by INVERTER, NAND, and NOR gates.

The standard deviation of the L and the VTO of the IC design are modeled by using Equations 1 and 2. By using these equations, the L and the VTO variations of the IC design are determined by Equations 3 and 4 subsequently.

$$\sigma_L = (n\% \cdot L) \quad (1)$$

$$\sigma_{VTO} = (n\% \cdot VTO) \quad (2)$$

$$VTO_n = VTO + gauss\ (\sigma_{VTO}) \quad (3)$$

$$L_n = L + gauss\ (\sigma_L) \quad (4)$$

Moreover, an evaluation method is proposed to evaluate the effects of the L and the VTO variation in *IC#i* by using a Monte Carlo SPICE simulation for measuring a quiescent supply current IDDQ. The simulation results are compared to the proposed IDDQ testing result [11] of a faulty IC. The faulty IC is illustrated in Figure 3, caused by an open defect inside it. The large quiescent supply current IDDQ will flow to the IC caused by the open defect.

Tolerance ranges of the *L* and the *VTO* variations in *IC#i* are determined by comparing their quiescent supply current IDDQ results to the IDDQ testing result [11]. *IC#i* may be detected

as defective IC by flowing the quiescent supply currents IDDQ being equal or larger than [11]. Hence, the maximum tolerance ranges of the L and the VTO variations are determined by the quiescent supply current IDDQ results are lower than [11].

3. Results ad Discussions

A simulation circuit was made to detect a faulty CMOS IC by using an IDDQ testing [11]. The circuit is presented in Figure 4, made by two ICs, *IC#*1 and *IC#*2. The *IC#*2 is a DUT (Device Under Test) of the faulty IC. The faulty is caused by an open defect denoted as "*a*" occurring inside the IC#2.

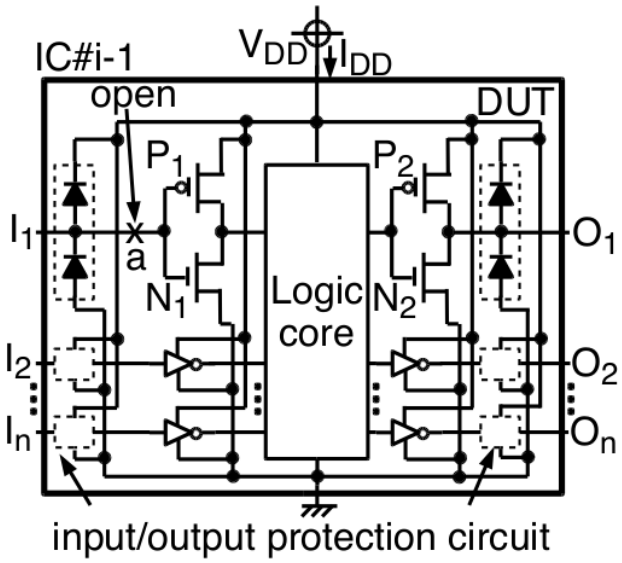


Figure 3. Faulty IC [11]

Both the ICs are designed using a SPICE Netlist Library distributed by NXP Co. Ltd. The ICs are an identical to a HCMOS IC design as shown in Figure 2. A NOR gate is used as a logic core in each the IC, so the functional ICs are as NAND gates.

A supply voltage V_{DD} is provided to the ICs by 3.3 V. The open defect is made by inserting a resistor 1 TΩ to *a*. The testing is based on measuring a quiescent supply current IDDQ of the ICs. The simulation result in Figure 5 shows large quiescent supply current IDDQ flowing to the ICs causing open defect. By using this phenomenon, an IC is detected as a faulty by flowing a large quiescent supply current IDDQ to it.

In order to evaluate the effects of L and VTO variations in a HCMOS IC, the simulation of circuit one is proposed and shown in Figure 6. The circuit is identical to the circuit in Figure 4; however, there is no detected defect. L and VTO variations of the circuit are modeled by modifying the SPICE Netlist Library using Equations 1 to 4.

Furthermore, the circuit in Figure 6 is simulated by a Monte Carlo SPICE simulation of LTSpice IV. The quiescent supply currents I_{DDQ} are measured to evaluate the effects of L and VTO variations. The I_{DDQ} values are compared to the proposed I_{DDQ} values [11]. When the I_{DDQ} values are equal or larger than them, the IC is detected as a faulty IC. The simulation results of *L* and VTO variations are shown in Figures 7 and 8 respectively.

As shown in Figure 7(a), I_{DDQ} values are less than 0.75 mA by using $\sigma_L = (18\% \cdot L)$. On the other hand, in Figure 7(b), with $\sigma_L = (19\% \cdot L)$, I_{DDQ} values are larger than 0.75 mA or equal to the I_{DDQ} values [10]. Therefore, a maximum standard deviation of *L* variations is $\sigma_L = (18\% \cdot L)$.

Moreover, in Figure 8 (a), by using $\sigma_{VTO} = (60\% \cdot VTO)$, I_{DDQ} values are less than 0.75 mA. However, in Figure 8(b), I_{DDQ} values are larger than 0.75 mA or equal to the I_{DDQ} values [11] with $\sigma_{VTO} = (70\% \cdot L)$. Moreover, $\sigma_{VTO} = (60\% \cdot VTO)$ is a maximum standard deviation of the *VTO* variations.

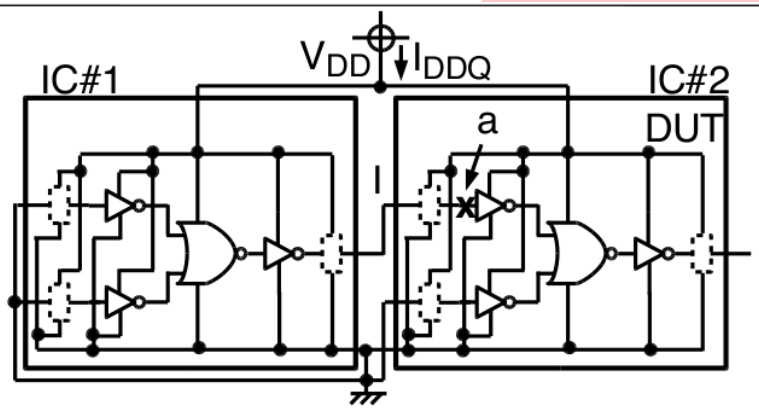


Figure 4. Simulation Circuit of Faulty IC

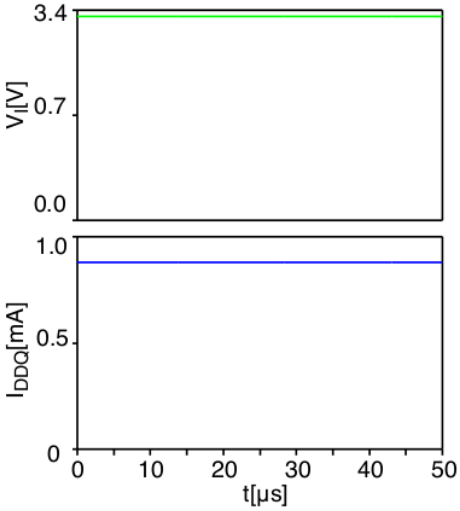


Figure 5. Simulation Circuit of Faulty IC

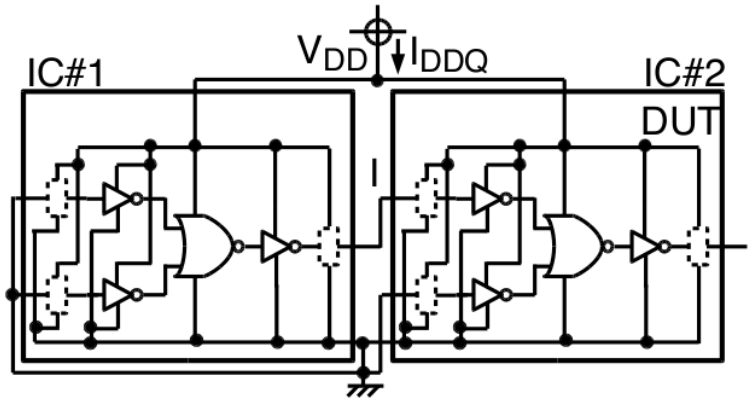
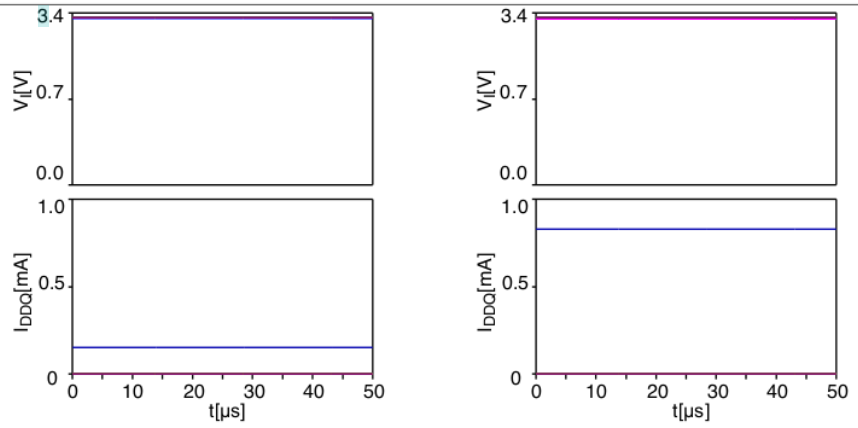
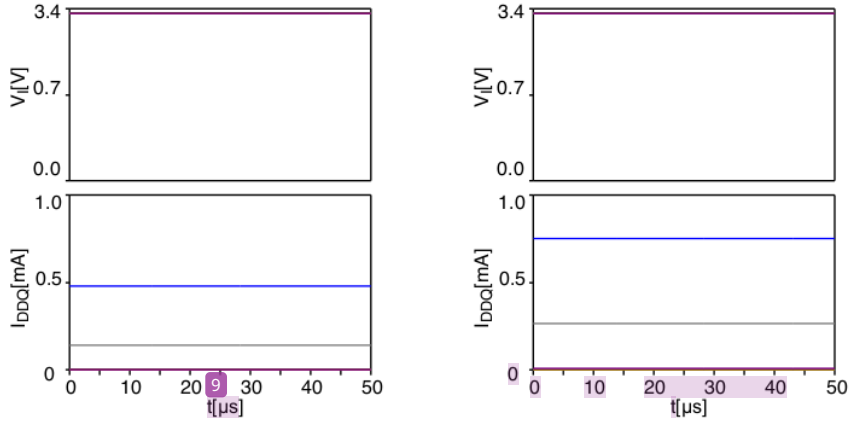


Figure 6. Simulation Circuit of Process Variation



(a) $\sigma_L = (18\% \cdot L)$ (b) $\sigma_L = (19\% \cdot L)$

Figure 7. Simulation Results of L Variations



(a) $\sigma_{VTO} = (60\% \cdot VTO)$ (b) $\sigma_{VTO} = (70\% \cdot VTO)$

Figure 8. Simulation Results of VTO Variations

4. Conclusion

The effects of process variations in a HCMOS IC are evaluated by using a Monte Carlo SPICE simulation of LTSpice IV. The process variations are L and VTO variations and modeled by a Gaussian distribution.

The simulation results show that maximum standard deviations of *L* and *VTO* variations are $\sigma_L = (18\% \cdot L)$ and $\sigma_{VTO} = (60\% \cdot VTO)$ respectively. Furthermore, it means that the maximum tolerance range of L variation is L ± (18%·*L*). However, VTO ± (60%·VTO) is the maximum tolerance range of *VTO* variation.

5. Notations

n : counting number
σ_L : standard deviation of L variation
σ_{VTO} : standard deviation of VTO variation

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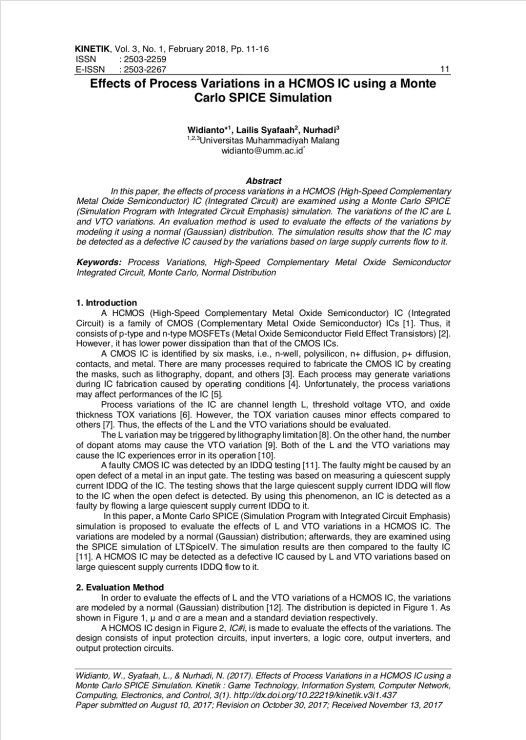

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