A SIGNATURE REGISTER OF A BIST TO DETECT STUCK- AT-FAULTS IN COMBINATIONAL LOGIC ICS

by Widianto Widianto

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A SIGNATURE REGISTER OF A BIST TO DETECT STUCK-AT-FAULTS IN COMBINATIONAL LOGIC ICS

Widianto[1], Robert Lis[2]
[1]University of Muhammadiyah Malang, Indonesia
[2]Wroclaw University of Science and Technology, Poland

Contact Person:
Widianto
Jl. Raya Tlogomas No. 246 Malang, Telepon: 0341-4641819 Fax: 0341-460782
E-mail: widianto@umm.ac.id

Abstract

A specific functionality of combinational logic ICs (integrated circuits) may become errors caused by occurring stuck-at-faults at its inputs and output logic gates. The faults may be detected by a signature register of a BIST (built-in self test). A circuit simulation of it is designed by Verilog. Moreover, as a CUT (circuit under test) is a combinational IC of XXX855 manufactured by Nexperia Semiconductor Company. A testability of the circuit is simulated using QuestaSim simulator. Simulation results show that the circuit may detect the faults occurring in the CUT.

Keywords: *stuck-at-faults, signature analyzer, BIST, combinational logic ICs*

1. Introduction

During fabrication processes, inputs and output logic gates consisting combinational logic ICs (integrated circuits) occurred by stuck-at faults [1],[2]. Specific functions of the ICs may become errors caused by the faults [3]. Therefore, the faults should be detected before.

The faults are a stuck-at-0 and a stuck-at-1[4]. The stuck-at-0 means connected either the input or the output logic gate to a ground and causes the gate become 0 value. On the other hand, the stuck-at-1 becoming the gate is 1 value caused by connected it to a supply voltage.

The faults in the logic gates of the ICs may not be detected by IDDQ testing [5],[6]. In the testing, a defect-free IC is measured by flowing a small quiescent supply current to it. However, the faults may cause logic values of the gates are either 1 or 0 values, the small quiescent currents will flow to the ICs.

A logic verification is a test to verify correctness functions of the ICs [7]. For example, using the logic verification to test an inverter logic IC may invert a provided signal or not. The such IC may not invert the provided signal caused by the faults.

A BIST (built-in self test) is the verification logic mechanism to test an IC by itself without adding an external hardware [8]. Occurring the faults inside the IC may be detected earlier by utilizing the BIST.

Occurring the faults inside a combinational logic IC may be detected by a BIST [9]. A test pattern generator signal is embedded inside the IC and is used to provide signals to the gates. Moreover, each response generated by the gates is analyzed one by one. Certainly, detecting the faults might a long test time.

A BIST implementing a signature analyzer signal was proposed to reduce a test time in detecting the faults. The faults may be detected by measuring signals generated by the analyzer [10]. However, one output of a combinational logic gate needs to be connected to one signature analyzer circuit. It means that a number of the analyzer circuit depends on output numbers of the logic gate. Therefore, it is required a large space to design it.

A signature register of a BIST is proposed to reduce a required space in[10]. Each output of a combinational logic gate is connected to one signature register. A Verilog is used to design a circuit simulation of it. Moreover, a testability of the circuit in detecting the faults is simulated using a Questasim simulator. Simulation results show utilizing the register of the BIST to detect the faults.

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2. Research Method

A BIST was used to detect stuck-at-faults in a combinational logic gate [9]. It consists LFSR (Linear Feed Back Shift Register). Each response generated by the gate is analyzed one by one in order to detect the faults. Of course, a long test time might need for detecting them.

Stuck-at-faults in a combinational logic gate were detected by utilizing a signature analyzer circuit of a BIST [10]. The faults are detected by observing generated signals of the circuit. However, it might require a large space since each output of the gate should be connected to one circuit.

Figure 1 shows a proposed BIST. A *PG* (pattern generator), a *SG* (signature register), multiplexers, *Mi*0 to *Mi*n, and de-multiplexers, *Mo*0 to *Mo*n, are consists of it. Furthermore, it is embedded inside a CUT of a combinational logic gate.

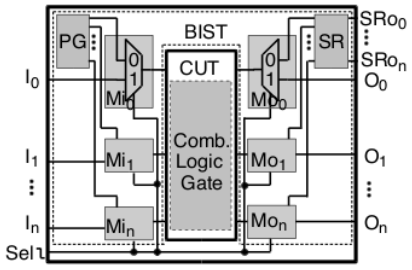
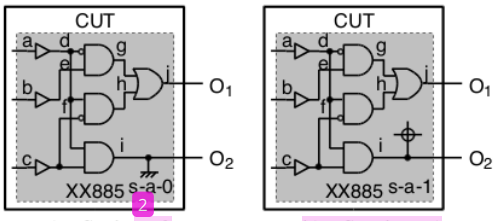


Figure 1 BIST circuit

Each of the multiplexers is two inputs-one output. However, one input-two outputs is each consist of de-multiplexers. Input numbers of the CUT are related to numbers of the multiplexers. Numbers of de-multiplexers are related to output numbers of the CUT. Moreover, a selector *Sel* of the multiplexers and de-multiplexers is used to select the BIST working either in a test mode or a normal mode is selected by.

To derive the test mode, a low logic signal is provided to the *Sel*. Generated signals of the PG will be propagated to the CUT and analyzed to the SR. Stuck-at-faults which occur at input and output logic gates consisting the combinational logic gate inside the CUT will be detected by observing outputted signals of the SR, *SRo*0 to *SRo*n.

The stuck-at-faults are a stuck-at-0 (s-a-0) and a stuck-at-1 (s-a-1) and are shown in Figure 2. In Figure 2a, occurring the s-a-0 at an output gate of a node *i* inside a CUT may cause a logic value of an output CUT *O*2 is stuck at a low logic value and input logic gate values of nodes c and a will be neglected. However, in Figure 2b, occurring the s-a-1 at the node *i* may cause the *O*2 is stuck at a high logic value.



a) Stuk-at-0 b) Stuck-at-1

Figure 2 Stuck-at-faults

The BIST is selected to the normal mode by providing a high logic signal to the Sel. Provided signals from input digital logics, *I*0 to *I*n, will be propagated to the CUT. Then, the signals are delivered to output digital logics, *O*0 to *O*n.

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The PG consisted by D Flip-Flops (DFFs) and an XOR gate. It is depicted in Figure 3. Numbers of the DFFs are related to numbers of the multiplexers. Connecting each output of the DFFs is to each one of the multiplexer inputs, *Mi*1 to *Mi*n. Furthermore, signals generated by the PG are a sequence signal of bits providing to the CUT. The signal is synchronized by a clock *clk* and initialized by a reset *rst*.

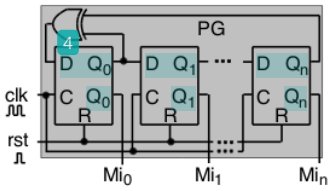

Figure 3 *PG* Circuit

D-FFs and XOR gates are consisted to design the SR. It is shown in Figure 4. The de-multiplexer numbers are related to numbers of the DFFs. Each output of the de-multiplexers, *Mo*0 to *Mo*n, is connected to each input of the SR. Propagated signals of the SR are a sequence signal of bits and used to analyze whether occurring the stuck-at-faults in the CUT or not. The signal is synchronized by the *clk*. Furthermore, it is initialized by the *rst*.

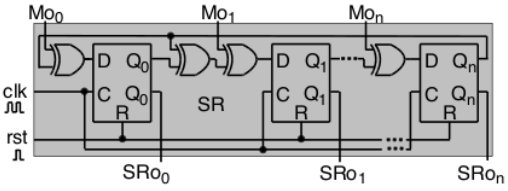

Figure 4 *SR* Circuit

3. Results and Discussion

A simulation circuit is shown in Figure 5 and is designed by a Verilog high description language. It consists of a PG, a SR, three multiplexers, two de-multiplexers, and a CUT. As the CUT is a combinational logic gate of XX885 manufactured by Nexperia Semiconductor Company. In order to test a feasibility of the circuit in detecting stuck-at-faults occurring inside the CUT, it is simulated using a QuestaSim simulator. A targeted fault is an output gate of a node *i* inside the CUT by a stuck-at-1.

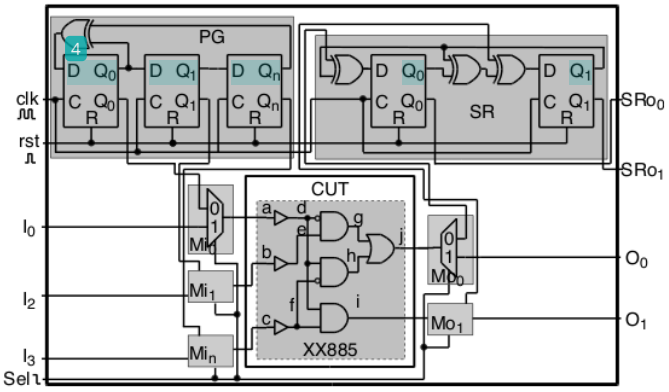

Figure 5 Simulation Circuit

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The circuit may work in either a normal or a test mode. The normal and the test mode are derived by providing a high and a low signal to a selector *Sel*, respectively. In the normal mode, provided signals of input digitals, *I*0 to *I*2, are propagated to the CUT. Then, the signals are delivered to output digitals, *O*0 and *O*1. Figure 6 is a simulation result of the normal mode.

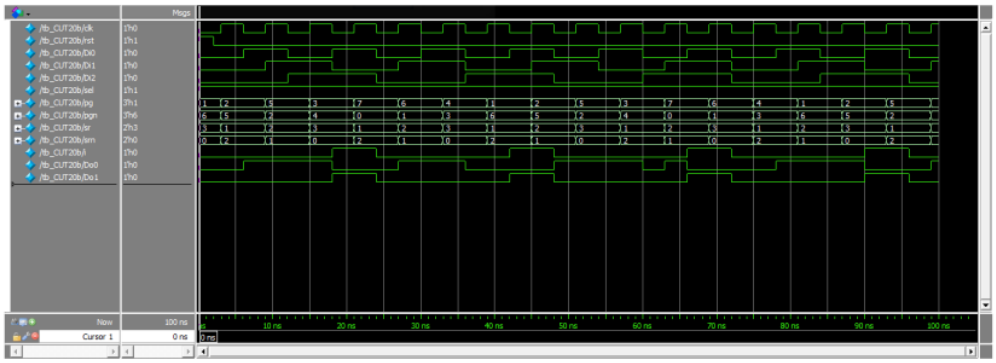

Figure 6 Normal Mode Result

A sample simulation time of the normal at 12 – 15 ns is shown in Figure 7. Provided signals by the $I0 = 0$, $I1 = 1$, and $I2 = 1$ are propagated to the CUT nodes a, b, and c, respectively. Then, the signals may cause $O0 = 1$, and $O1 = 0$.

```
# T=12, clk=0, rst=0, pg=101, pgn=010, I0=0, I1=1, I2= 1, sel=1, O0=1, O1=0, i=0, sr=10, srn=01
# T=15, clk=1, rst=0, pg=011, pgn=100, I0=0, I1=1, I2= 1, sel=1, O0=1, O1=0, i=0, sr=11, srn=00
```

Figure 7 Sample Simulation Time of Normal Mode

In the test mode, the signals of *I*0 to *I*2 will be neglected. Providing a high signal to a reset *rst* is used to initialize a signal of the circuit. Moreover, it is synchronized by providing a pulse wave signal to a clock *clk*. Each positive edge signal of the *clk* may trigger a change of each output signal generated by the PG and the SR. Generated signals of the *PG* are propagated to the *CUT* and observed to the *SR*, *SRo*0 and *SRo*1. The *SR* is used to analyze either the faults occurring inside the CUT or not.

Figure 8 is a simulation result of a fault-free circuit. Furthermore, a sample simulation time of the fault-free circuit at 12 – 15 ns is shown in Figure 9. Generated signals by the PG of *pgn* are 010 and 011. For example, when the *pgn* signals are 011 at the time $T = 15$ ns, they mean that the CUT nodes $a = 0$, $b = 1$, and $c = 1$. Such signals may cause the CUT node $i = 0$ and two outputs the SR, $SRo0 = 0$ and $SRo1 = 1$.

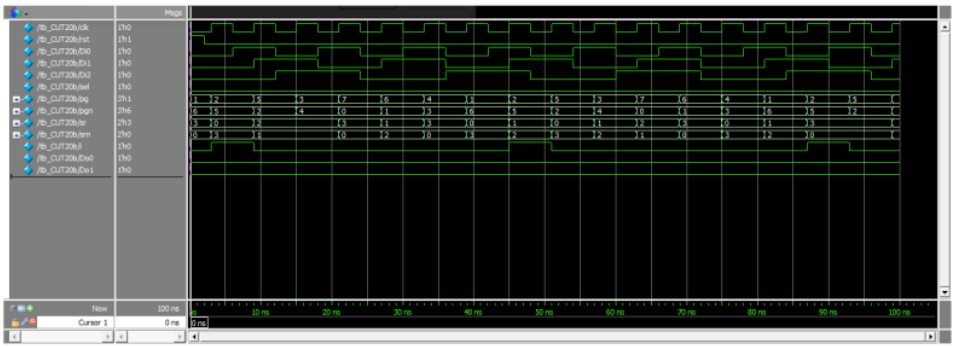

Figure 8 Fault-free Result

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```
# T=12, clk=0, rst=0, pg=101, pgn=010, I0=0, I1=1, I2= 1, sel=0, O0=0, O1=0, i=0, sr=10, srn=01
# T=15, clk=1, rst=0, pg=011, pgn=100, I0=0, I1=1, I2= 1, sel=0, O0=0, O1=0, i=0, sr=10, srn=01
```

Figure 9 Sample Simulation Time of Fault-free Circuit

The CUT node *i* is the targeted fault of the stuck-at-1 by inserting a high signal to a sample simulation time at 12 – 15 ns. Figure 10 is a simulation result of a faulty circuit. Generated signals by the PG are neglected at the time, the signal of the node *i* is stuck at the high signal. The fault is detected by analyzing the outputted signal of $SRo0 = 1$ and $SRo1 = 1$ at the time $T = 15$ ns compared with the fault-free result at the same time. Figure 11 shows the sample simulation time of the faulty circuit.

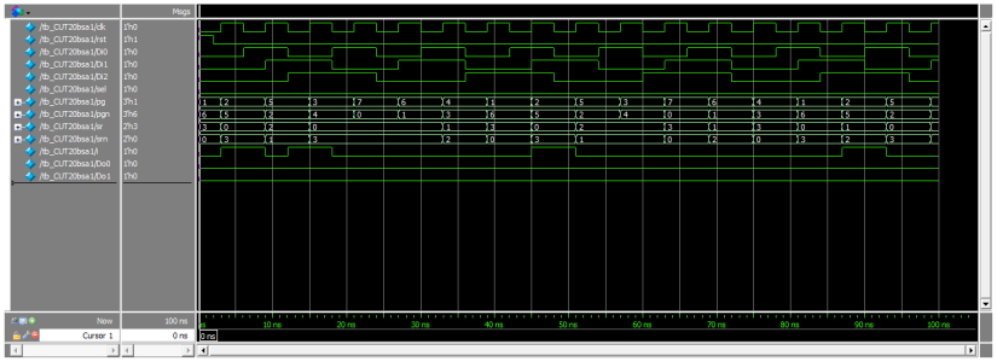

Figure 10 Faulty Result

```
# T=12, clk=0, rst=0, pg=101, pgn=010, Di0=0, Di1=1, Di2= 1, sel=0, Do0=0, Do1=0, i=1, sr=10, srn=01
# T=15, clk=1, rst=0, pg=011, pgn=100, Di0=0, Di1=1, Di2= 1, sel=0, Do0=0, Do1=0, i=1, sr=00, srn=11
```

Figure 11 Sample Simulation Time of Faulty Circuit

4. Conclusion

Occurring stuck-at-faults at inputs and output gates consisting a combinational logic gate IC may be detected by utilizing a signature register of a BIST. In order to detect the faults, signals outputted by the register at a faulty circuit are compared to a fault-free circuit. If the signals are not equal at a same time simulation, it means that the faults may occur inside the circuit. In the future work, faults coverage of the built-in self test in detecting the faults should be increased.

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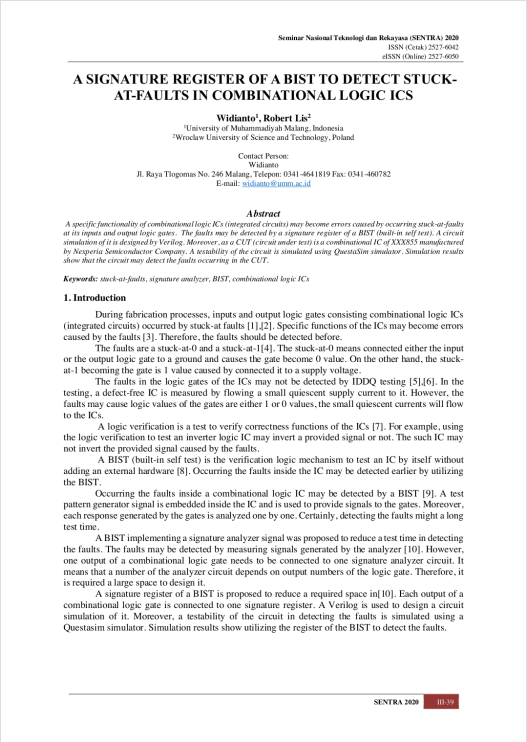

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