

IDDQ TESTING FOR DETECTING RESISTIVE OPEN DEFECTS IN HCMOS LOGIC ICs

Widianto*¹, Lailis Syafaah², Nurhadi³

^{1,2,3}University of Muhammadiyah Malang

Kontak person:

Widianto

e-mail: widianto@umm.ac.id¹

Abstract

Resistive open defects may occur at an input gate in a HCMOS logic IC. The defects may be caused by an opened metal line and may degrade performances of the IC. An IDDQ testing is proposed to detect the defects. The testing is based on measuring a quiescent supply current IDDQ value which flows to the IC. The defective IC is detected by flowing the larger IDDQ value compared to the defect-free IC. Feasibility of the testing is implemented in the IC designed by a SPICE library of NXP semiconductor Co. Ltd and is examined using a SPICE simulation of LTSpiceIV. Simulation results show that the resistive open defects may be detected by the IDDQ testing.

Keywords: resistive open defects, HCMOS IC, IDDQ testing, defective IC

1. Introduction

In an IC (integrated circuits) technology related to Moore law's, a speed of ICs will increase doubled roughly every 34 months[1]. A mentioned phenomenon may occur in CMOS (complementary metal oxide semiconductor) ICs which develop to HCMOS (high speed CMOS) ICs. However, open defects may occur inside the CMOS ICs as well as the HCMOS ICs by opened input gates[2]. Thus, the defects should be tested before shipping the HCMOS ICs to be delivered to customers.

The open defects are opens at metal lines. They are caused by the increasing number contacts and vias[3]. The open defects may differentiate into two parts, i.e. a hard open defect and a resistive open defect. The hard open defect disconnects fully the metal lines. On the other hand, the metal lines are disconnected partially by the resistive open defect.

The hard open defect inside the ICs can be detected by an I_{DDQ} testing based measuring its quiescent supply current[4]. The quiescent supply current IDDQ of the ICs by the open defect will be larger compared to defect-free ICs. However, test input vectors should be determined earlier to detect the defect.

An IDDQ testing regardless generated test input vectors was proposed to detect the hard open defect[5]. A DUT of the IC was made to evaluate feasibility of the testing in detecting the defect. However, in the proposed DUT, the resistive open defect may not be detected by the testing. Thus, the DUT of the IC should be revised in order to detect the resistive open defect by the testing.

In this paper, an IDDQ testing by a new DUT is proposed to detect the resistive open defect. In order to evaluate feasibility of the testing in detecting the resistive open defect, the DUT is examined using a SPICE simulation of LTSpiceIV. The DUT is made by a SPICE netlist library distributed by NXP Co. Ltd. Furthermore, analysis results are denoted in this paper.

2. Research Method

An IDDQ testing is proposed to detect resistive open defects in a HCMOS IC. The testable DUT (device under test) IC is shown in Figure 1. The IC consists of input pins I1 to In, output pins O1 to On, and a supply voltage pin VDD. Furthermore, it is made of protection circuits, inverters, and a logic core. The logic core may be inverter, NAND, NOR, and other logic gates. A targeted resistive open defect is denoted as "a" in the IC. The IDDQ testing may detect the targeted defect by measuring a quiescent supply current IDDQ of the IC.

For an example, an inverter gate is used as the logic core. Electrical characteristics of the inverter gate are shown in Fig. 2. As shown in Fig. 2(b), when an input voltage of the gate V_i is a H or a L level, supply current i_{DD} of almost zero will flow into the gate. On the other hand, if V_i is in a range specified by Eq. (1), large i_{DD} will flow, since both a pMOS P_1 and an nMOS N_1 in the gate turn on.

When a resistive open defect occurs at the targeted a , a large quiescent supply current IDDQ flows to the IC, regardless either a H or a L level signal is provided to an input pin of the IC I_1 , since the input voltage of the inverter as the logic core is the range specified by Eq. (1). However, in the defect-

free IC, the I_{DDQ} is almost zero will flow to the IC, when the input voltage of the inverter is either a H or a L level signal.

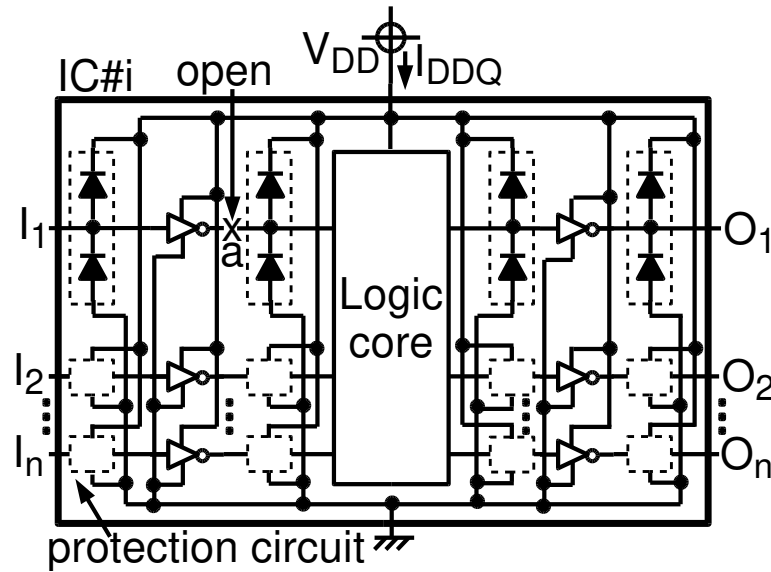
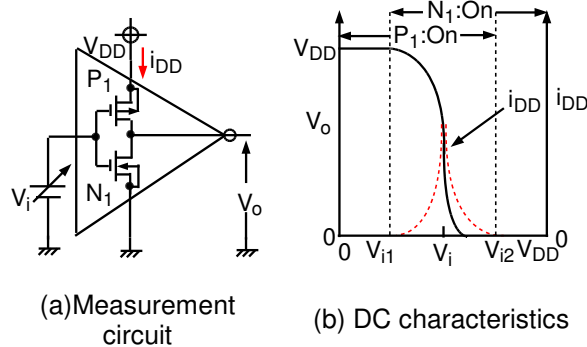


Figure 1. DUT IC

$$V_{i1} \leq V_i \leq V_{i2} \quad (1)$$



(a) Measurement circuit

(b) DC characteristics

Figure 2. Electrical characteristics of inverter gate

3. Results and Discussion

In order to evaluate feasibility of an I_{DDQ} testing in detecting a resistive open defect which occurs at an input gate of a HCMOS IC, a simulation circuit is made as shown in Figure 3. Two ICs, IC#1 and IC#2, are implemented in the circuit. A SPICE netlist library of NXP Co. Ltd is used to design both the ICs. IC#2 is a DUT which denoted "a" as a targeted resistive open defect.

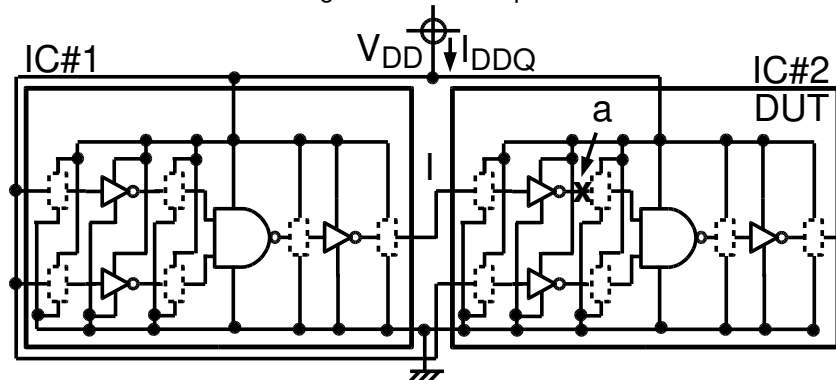


Figure 3. Simulation circuit

A supply voltage V_{DD} and a are provided by 3.3 V and a resistor 100 G Ω , respectively. Moreover, the circuit is simulated using a SPICE simulation of LTSpiceIV. It is tested using the IDDQ testing by measuring a quiescent supply current IDDQ. Simulation results are shown in Figure 4. In defect-free ICs, the IDDQ is almost zero flows to the circuit as shown in Figure 4(a). In Figure 4(b), the defective circuit caused by the resistive open defect in the targeted a is detected by flowing the large IDDQ.

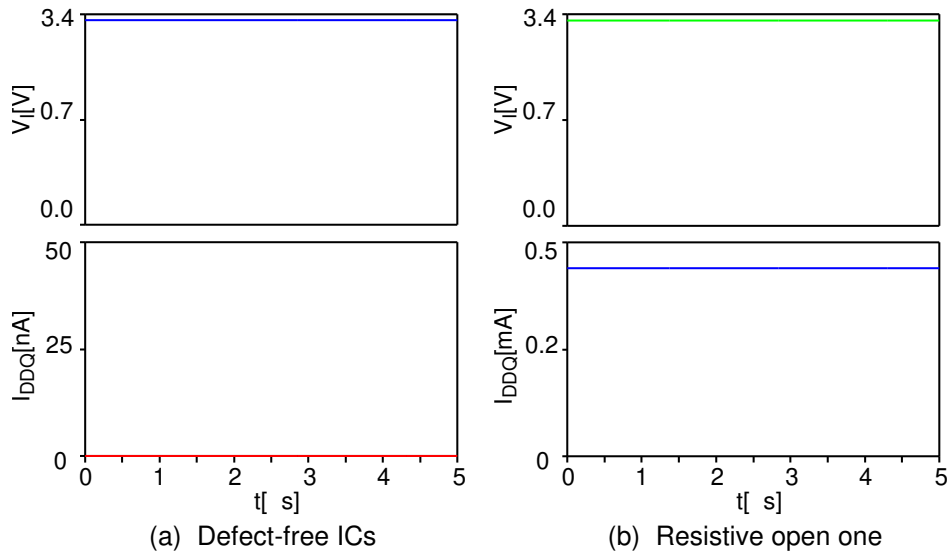


Figure 4. Simulation results

4. Conclusion

A resistive open defect occurring in an input gate of a HCMOS IC may be detected using an IDDQ testing. The testing is based on measuring a quiescent supply current IDDQ of the IC. The resistive open defect is detected by flowing the larger IDDQ compared to the defect-free IC. In order to locate the defect, it is a future work.

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