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Abstract. Open defects may occur at interconnection between gates inside HCMOS logic ICs due to open metal at imperfect fabrication process affecting speed responses of the ICs. A SPICE simulation is thus proposed to analyze delays due to the defects inside the ICs. The ICs are designed from a HCMOS netlist library distributed by Nexperia Co. Ltd. Simulation results indicate that the delays linearly increase along with sizes and locations of the defects.

INTRODUCTION

A HCMOS (High-Speed Complementary Metal Oxide Semiconductor) logic IC (Integrated Circuit) is regarded under a family of CMOS ICs [1]. Thus, it is made of p-type and n-type MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) [2], with a higher speed response than that in the CMOS ICs.

There are six masks in fabrication process of the HCMOS IC, which are: n-well, polysilicon, n+ diffusion, p+ diffusion, contact, and metal [3], specifying the proper placement of the transistor by layout designed rules [4] describing the scalable width and spacing for each step of the masks.

The HCMOS IC contains a logic diagram where some logic gates are connected to each other for specific function [5]. For instance, an inverter IC consists of the three inverter gates where the output gate one is connected to the other input gate and so on. The metal of the masks is utilized to connect each logic gate to others [6]. Construction of the parallel metal layer forms the capacitor with low capacitance values [7]. However, resistor is formed by series of metal layers along with resistance values depending on resistivity of the layer.

An open defect might thus occur at interconnection between logic gates [8] due to the open metal at the imperfect fabrication process. Moreover, the open defect in the metal might linearly increase along with the resistance values of the metal and the speed response of the IC.

The open defect between logic gates inside an IC was detected by an IDDQ testing [9], indicating that a large quiescent supply current will flow when the open defect occurs inside it. However, an ESD (Electronic Discharge) circuit should be added in each input gate requiring large space.

Delay testing is proposed to detect the open defects [10]. However, a test pattern should be prepared prior to testing logic IC one, requiring longer preparation time for different test patterns.

This study proposes a SPICE (Simulation Program with Integrated Circuit Emphasis) simulation of LTSpiceXVII to analyze delays in HCMOS logic gate ICs due to open defects. The ICs are designed by a HCMOS netlist library distributed by Nexperia Co. Ltd. The simulations results indicate that the delays in the IC are analyzed where the delay linearly increase along with sizes and locations of the defects.

METHODS

A HCMOS logic IC consists of a logic diagram with input voltages of *Vi*1 to *Vi*n, and output voltages of *Vo*1 to *Vo*n, depicted in Figure 1. The diagram presents different specific functions of the IC, which include: Inverter, NOR, and NAND as well as other logic gates, such as: an inverter logic IC constructed by the three inverter logic gates.

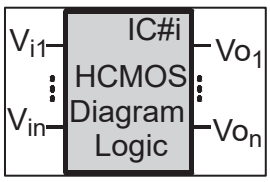

FIGURE 1. HCMOS IC Design

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Open defects occur at each input gate inside HCMOS logic ICs. For example, a logic diagram of an inverter logic IC is illustrated in Figure 2. As previously illustrated in Figure 1, the inverter IC has an input voltage of *Vi* and an output voltage of *Vo*. The open defect occurs inside the IC: *a*, b, and *c* nodes.

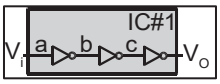


FIGURE 2. Inverter logic diagram

In the logic ICs, the defect generates the delays derived by providing stimulus signals to the IC inputs and by measuring time intervals between generated signals at IC outputs and its stimulus. The delays are divided into two types, which include: delay fall time *tdelayf* and delay rise time *tdelayr*.

The delay measurement of the inverter IC is illustrated in Figure 3, measured to time interval between generated signal waveform at *Vo* and stimulus signal waveform at *Vi*. As illustrated in Figure 1, *tdelayf* is measured to time interval between the move waveform from high level to low level signal reaching 50% at *Vo* and the move waveform from low level to high level reaching 50% at *Vi*. Moreover, measuring time interval between the move waveform from high level to low level signal reaches 50% at *Vo* and the move waveform from low level to high level reaches 50% at *Vi* is to derive *tdelayr*

Moreover, the defect might increase fall time *tfall* and rise time *trise* at generated signals of IC outputs. *tfall* measures time interval of the move waveform from high to low level signal. On the other hand, *trise* measures time interval of the move waveform from low to high level signal.

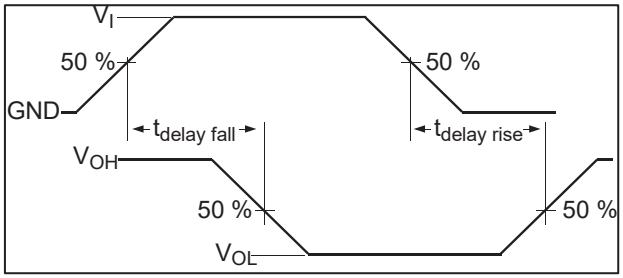


FIGURE 3. Measurement of delay time

Measuring *tfall* and *trise* of the inverter IC is illustrated in Figure 4. As illustrated in Figure 4, *tfall* presents time interval of the move waveform from 90% high to 10% low level signal. However, time interval of the move waveform from 10% low to 90% high signal is presented by *trise*.

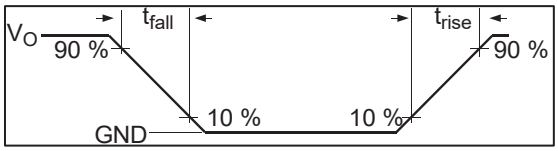


FIGURE 4. Measuring rise dan fall time

SPICE contains the facilities to measure *tdelayf*, *tdelayr*, *tfall*, and t*rise* in the HCMOS logic IC design by applying a command '.meas'. The delays are triggered *trig* at *Vi* and targeted *targ* at *Vo*. Syntaxes for measurement are illustrated in Figure 5.

```
.meas tdelayr trig V(Vil to Vin) = 0.5*(Vil to Vin) fall = count
targ V(Vol to Von) = 0.5*(Vol to Von) rise = count
.meas tdelayr trig V(Vil to Vin) = 0.5*(Vil to Vin) fall = count
targ V(Vol to Von) = 0.5*(Vol to Von) rise = count
.meas trise trig V(Vol to Von) = 0.1*(Vol to Von) rise = count
targ V(Vol to Von) = 0.9*(Vol to Von) rise = count
.meas tfall trig V(Vol to Von) = 0.9*(Vol to Von) fall = count targ
V(Vol to Von) = 0.1*(Vol to Von) fall = count
```

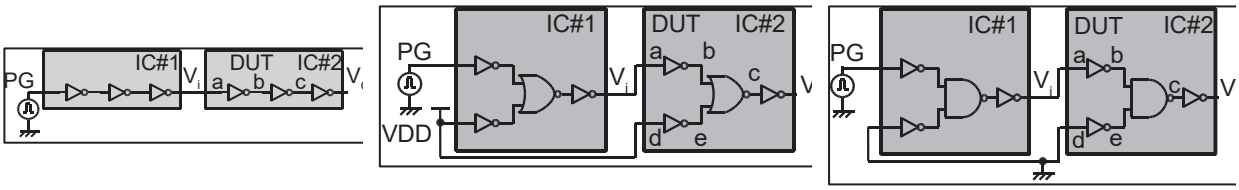
FIGURE 5. Syntaxes for measuring delay time

RESULTS AND DISCUSSION

This study analyzes the HCMOS logic ICs, NAND, and NOR By creating the simulation circuits due to open defects in the HCMOS logic ICs. The circuits of inverter, NAND, and NOR are illustrated in Figure 6a, 6b, and 6c respectively. Each the Figure consists of two ICs, IC#1 and IC#2. A PG (Pattern Generator) is provided to IC#1. IC#2 as a DUT (Design Under Test) which the delays are measured.

The inverter IC has three targeted open defects of a, b, and c. Moreover, the NOR and NAND ICs have five targeted defects, located at a, b, c, d, and e nodes. Resistors *Ropen* of 1 kΩ, 10 kΩ, 100k, 1 MΩ, 10 MΩ are inserted to the targeted defects. The delays are measured to time interval between generated signal waveform at output voltage *Vo* and stimulus signal waveform at input voltage *Vi.* The measured delays include *tdelayr* and *tdelayf* along with measuring *trise* and *tfall.*

Simulation results of defect-free ICs when signals moving from high to low (H-L) at Vo are summarized in Table 1. Moreover, Table 2 summarizes simulation results of defect-free ICs when signals move from low to high (L-H) at Vo.



a) Inverter IC b) NAND IC c) NOR IC

FIGURE 6. DUT of IC#2

TABLE 1. Defect-free ICs when Vo of H-L

IC	tdelayr (µs)	tdelayf (µs)	trise (µs)	tfall (µs)
NAND	0.001	0.004	0.000	0.002
NOR	0.001	0.001	0.000	0.000
INV	0.000	0.000	0.001	0.002

TABLE 2. Defect-free ICs when Vo of L-H

IC	tdelayr (µs)	tdelayf (µs)	trise (µs)	tfall (µs)
NAND	0.001	0.004	0.000	0.002
NOR	0.000	0.001	0.002	0.000
INV	0.001	0.002	0.000	0.000

Simulation results of defective ICs where Ropen is inserted to the located defects are summarized in Table 3 and 4. Table 3 summarizes the results at Vo of H-L, while the results at Vo of L-H are summarized in Table 4.

TABLE 3. Defective ICs at Vo of H-L

Location	Ropen (Ω)	tdelayr (µs)			tdelayf (µs)			trise (µs)			tfall (µs)		
		NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV
b	1 k	0.001	0.001	0.002	0.005	0.001	0.002	0.000	0.000	0.000	0.002	0.002	0.000
	10 k	0.003	0.004	0.007	0.009	0.002	0.006	0.000	0.000	0.001	0.001	0.000	0.000
	100 k	0.022	0.025	0.058	0.055	0.001	0.044	0.002	0.002	0.004	0.003	0.002	0.002
	1 M	0.192	0.229	0.563	0.495	0.001	0.405	0.013	0.013	0.023	0.013	0.001	0.015
	10 M	1.869	2.246	5.591	4.222	0.001	1.904	0.085	0.093	0.173	0.099	0.001	0.165
a	1 k	0.001	0.001	0.001	0.005	0.002	0.002	0.000	0.000	0.000	0.001	0.001	0.000
	10 k	0.005	0.005	0.003	0.011	0.002	0.003	0.000	0.000	0.000	0.001	0.000	0.000
	100 k	0.041	0.041	0.015	0.063	0.002	0.017	0.000	0.001	0.000	0.001	0.000	0.000
	1 M	0.387	0.392	0.119	0.582	0.002	0.141	0.003	0.002	0.001	0.002	0.000	0.001

Location	Ropen (Ω)	tdelayr (µs)			tdelayf (µs)			trise (µs)			tfall (µs)		
		NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV
	10 M	3.833	3.874	1.125	3.250	0.002	1.355	0.017	0.010	0.003	0.008	0.000	0.003
c	1 k	0.001	0.002	0.002	0.005	0.002	0.003	0.001	0.001	0.001	0.002	0.001	0.001
	10 k	0.010	0.011	0.011	0.020	0.017	0.018	0.008	0.009	0.008	0.009	0.009	0.008
	100 k	0.100	0.100	0.101	0.169	0.167	0.168	0.083	0.085	0.083	0.089	0.084	0.087
	1 M	0.999	0.999	0.999	1.659	1.654	1.656	0.802	0.803	0.800	0.812	0.811	0.810
	10 M	22.151	~	22.149	17.907	~	17.913	~	~	~	~	~	~
d	1 k	0.001	0.001		0.005	0.001		0.000	0.000		0.001	0.001	
	10 k	0.005	0.001		0.011	0.002		0.000	0.000		0.001	0.002	
	100 k	0.041	0.036		0.064	0.002		0.000	0.000		0.001	0.002	
	1 M	0.386	0.384		0.586	0.002		0.002	0.000		0.002	0.002	
	10 M	3.808	3.841		3.284	0.002		0.012	0.010		0.008	0.002	
e	1 k	0.001	0.001		0.005	0.001		0.000	0.000		0.002	0.002	
	10 k	0.003	0.001		0.010	0.002		0.000	0.000		0.001	0.002	
	100 k	0.023	0.018		0.054	0.002		0.002	0.002		0.003	0.002	
	1 M	0.206	0.207		0.484	0.002		0.013	0.013		0.015	0.002	
	10 M	2.013	2.078		4.150	0.002		0.088	0.086		0.136	0.002	

TABLE 4. Defective ICs at Vo of L-H

Location	Ropen (Ω)	tdelayr (µs)			tdelayf (µs)			trise (µs)			tfall (µs)		
		NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV
b	1 k	0.001	0.001	0.002	0.005	0.000	0.002	0.000	0.000	0.000	0.001	0.000	0.000
	10 k	0.003	0.003	0.007	0.009	0.001	0.006	0.000	0.002	0.000	0.002	0.002	0.000
	100 k	0.022	0.022	0.058	0.055	0.001	0.044	0.002	0.002	0.004	0.003	0.000	0.002
	1 M	0.192	0.203	0.563	0.495	0.001	0.405	0.014	0.013	0.023	0.013	0.000	0.015
	10 M	1.243	1.833	3.100	4.838	0.001	3.974	0.091	0.093	0.173	0.099	0.000	0.167
a	1 k	0.001	0.001	0.001	0.005	0.001	0.002	0.000	0.002	0.000	0.001	0.000	0.000
	10 k	0.005	0.005	0.003	0.011	0.001	0.003	0.000	0.002	0.000	0.001	0.000	0.000
	100 k	0.041	0.041	0.015	0.063	0.001	0.017	0.000	0.001	0.000	0.001	0.001	0.000
	1 M	0.387	0.392	0.119	0.582	0.001	0.141	0.003	0.002	0.001	0.002	0.000	0.001
	10 M	1.764	1.804	1.121	5.742	0.001	1.365	0.019	0.010	0.003	0.008	0.000	0.003
c	1 k	0.001	0.002	0.002	0.005	0.002	0.003	0.001	0.001	0.001	0.002	0.001	0.001
	10 k	0.010	0.011	0.011	0.020	0.016	0.018	0.008	0.008	0.008	0.009	0.009	0.008
	100 k	0.100	0.100	0.101	0.169	0.167	0.168	0.085	0.093	0.086	0.089	0.086	0.088
	1 M	0.992	0.991	0.992	1.674	1.674	1.674	0.802	0.800	0.799	0.813	0.811	0.810
	10 M	~	~	~	~	~	~	~	~	~	~	~	~
d	1 k	0.002	0.001		0.005	0.001		0.000	0.000		0.002	0.002	
	10 k	0.005	0.003		0.011	0.002		0.000	0.000		0.002	0.002	

Location	Ropen (Ω)	tdelayr (µs)			tdelayf (µs)			trise (µs)			tfall (µs)		
		NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV	NAND	NOR	INV
	100 k	0.041	0.039		0.064	0.002		0.000	0.000		0.001	0.002	
	1 M	0.386	0.387		0.586	0.002		0.002	0.002		0.002	0.001	
	10 M	1.739	1.774		5.776	0.002		0.012	0.010		0.009	0.001	
	1 k	0.001	0.001		0.005	0.001		0.000	0.000		0.001	0.002	
	10 k	0.003	0.002		0.010	0.002		0.000	0.000		0.003	0.002	
e	100 k	0.023	0.020		0.054	0.002		0.002	0.002		0.003	0.002	
	1 M	0.206	0.192		0.484	0.002		0.014	0.012		0.015	0.000	
	10 M	1.326	1.325		4.739	0.002		0.098	0.093		0.136	0.002	

CONCLUSIONS

A SPICE simulation was proposed in this study to analyze delays due to open defects at interconnection between gate inside HCMOS logic ICs. The measured delays are *tdelayr* and *tdelayf*,, *trise* and *tfall.* The simulation results indicate that the delays linearly increase along with sizes and locations of the defects.

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