Build Testbenches for Verification in Shift Register ICs using SystemVerilog

by Widianto Widianto

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Build Testbenches for Verification in Shift Register ICs using SystemVerilog

Widianto, M. Chasrun H., and Robert Lis

***Abstract*—A testbench is built to verify a functionality of a shift register IC (Integrated Circuit) from stuck-at-faults, stuck-at-1 as well as stuck-at-0. The testbench is supported by components, i.e., generator, interface, driver, monitor, scoreboard, environment, test, and testbench top. The IC consists of sequential logic circuits of D-type flip-flops. The faults may occur at interconnects between the circuits inside the IC. In order to examine the functionality from the faults, both the testbench and the IC are designed using SystemVerilog and simulated using Questasim simulator. Simulation results show the faults may be detected by the testbench. Moreover, the detected faults may be indicated by error statements in transcript results of the simulator.**

***Keywords*—testbench; verification; shift register IC; stuck-at-faults; SystemVerilog**

I. Introduction

SHIFT register Integrated Circuits (ICs) may be applicated to serial-to-parallel data conversion and remote control holding register[1]. The ICs may be implemented to displays and control units. They consist of sequential logic circuits, i.e. D-type flip-flops. Stuck-at-faults may occur at either inputs or output interconnects between the circuits inside the ICs[2].

The faults may be caused by shorted the interconnects to supply voltage (stuck-at-1) and ground (stuck-at-0)[3]–[5]. The inputs and outputs of the circuits may stick at high and low values caused by the stuck-at-1 and stuck-at-0, respectively. Since the faults may cause functions of the ICs become errors, they should be detected.

The faults may be detected by an Automatic Test Pattern Generation (ATPG)[6]–[9]. However, it needs to integrate the external tools and programs where integrating them is not easy. Furthermore, it requires a circuit partitioning and a bit parallel processing.

A Built-in Self Test (BIST) was proposed to detect the faults[10]–[12]. The BIST consisted by a signature analyzer[13]. The analyzer is used to compare signals generated by the faults and faults-free and further analyze them. However, it takes time consuming, since the signal faults are detected by checking the generated signals one-by-one. Furthermore, the BIST is still designed by a Verilog Hardware Description Languages (HDL) in which it isn't supported by Object Oriented Programming (OOP) features[14]–[16], thus the detected faults aren't indicated by pass/ error statements.

A SystemVerilog is an extension of the Verilog HDL[17]–[21] used to design and verify hardware[22][23], e.g., Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). The hardware design is created in a Register Transfer Level (RTL) model. Moreover, to verify functionality of the design working as expected, a testbench should be built[24]. The testbench drives different input stimulus to the design and is supported by the OOP features.

In this paper, a proposed shift register IC is designed using the SystemVerilog. It will be verified the functionality from both stuck-at-faults, stuck-at-1 and stuck-at-0 by a testbench. The designed IC and its testbench are simulated using Questasim simulator[25]. Simulation results denote that the faults inside the IC may be detected by the testbench. Furthermore, indicating pass/ error statements is included in the detected faults by it.

II. Research Method

A testbench is built to verify a functionality of a shift register IC from both stuck-at-faults, stuck-at-1 and stuck-at-0. The testbench architecture is shown in Figure 1. There are some supported components, namely, transaction object, generator, interface, driver, monitor, scoreboard, environment, test, and testbench top. The IC is as a Design Under Test (DUT).

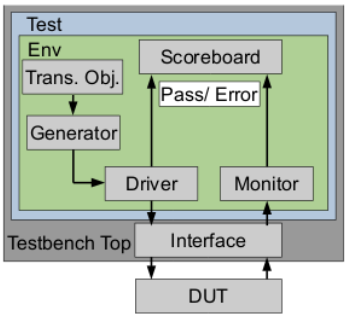

Fig.1. Testbench architecture

The DUT is a sample 8-bit shift register IC produced by Nexperia Co. Ltd. A logic diagram of the DUT is shown in Figure 2. As shown in Figure 2, the DUT consists of four buffer gates, two inverter gates, and eight stages, stage 0 to stage 7. Each of the stages is made of a buffer gate and two D flip-flop types in which the D flip-flop types are a shift register *sh* and a storage register *st*. Symbol descriptions in the DUT are shown in Table I.

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First Author and Second Author are with University of Muhammadiyah Malang, Department of Electrical Engineering, Indonesia (e-mail: widianto@umm.ac.id and chasrun@umm.ac.id)

Third Author is with Wroclaw University of Science and Technology, Poland (e-mail: Robert.lis@pwr.edu)

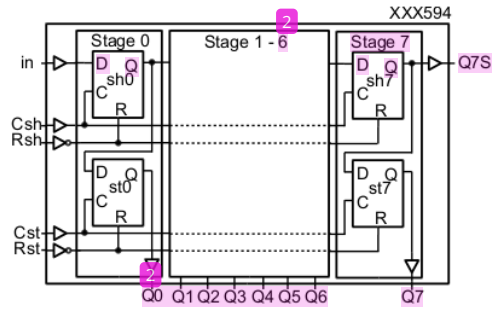


Fig.2. Logic diagram of the DUT

TABLE I
SYMBOL DESCRIPTION OF THE DUT

Symbol	Description
in	Serial data input
Csh	Shift register clock input
Rsh	Shift register reset input
Rst	Storage register reset input
Q0-to-Q7	Parallel data output
Q7S	Serial data output

Moreover, the DUT is designed using a SystemVerilog. The SystemVerilog code of the DUT is shown in Figure 3. The code is based on logic diagram as shown in Figure 2. There are eight stages, four inverters, and two inverters in the code.

```
module sh594b (in, Csh, Rsh, Cst, Rst, Q, Q7S, qsh);
input in, Csh, Rsh, Cst, Rst;
output [7:0] Q;
output Q7S;
output [7:0] qsh;

inva u3 (.g(rsh), .f(Rsh));
 …
stage u5 (.dsh(dsh), .csh(csh), .rsh(rsh), .cst(cst), .rst(rst),
.qsh(qsh[0]), .qst(Q0));
…
buff u13 (.d(Q7S), .c(qsh[7]));

assign Q = {Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0};

endmodule
```

Fig.3. SytemVerilog code of the DUT

A timing diagram of the DUT is shown in Figure 4. The DUT is reset by providing low level signals to the *Rsh* and the *Rst*. If the DUT is reset, all outputs of the Q7S and the *Q*0-to-*Q*7 are low level signals.

On the other hand, the DUT will run by providing high signals to the *Rsh* and the *Rst*. When a high pulse and clock signals are provided to the *in* and the *Csh*, respectively, the pulse signal will be shifted to each the stage and outputted serially to the Q7S since low-to-high transitions of the *Csh*. Moreover, clock signals are provided to the *Cst* behind one clock pulse of the *Csh*, the pulse signal will be shifted parallelly to the *Q*0-to-*Q*7 when low-to-high transitions of the *Cst*.

Stuck-at-faults may occur at interconnects between the stages inside the DUT. For example, Figure 5a shows a stuck-at-1 occurring between the stage 0 and the stage 1. The stuck-at-1 may cause an output of the *sh*0 in the stage 0 will stick at a high level signal regardless provided level signals of the *in*. On the other hand, occurring a stuck-at-0 is shown in Figure 5b. An output of the *sh*0 in the stage 0 will stick at a low level signal caused by the stuck-at-0.

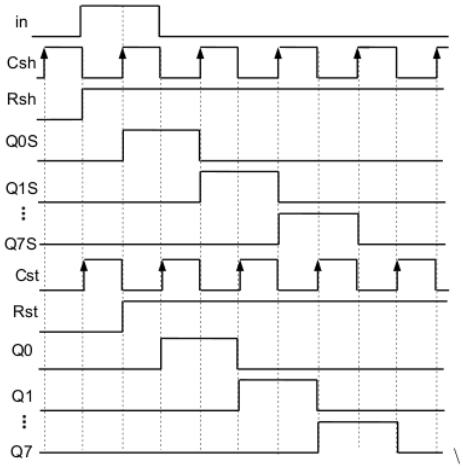
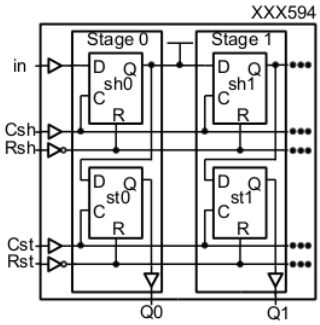
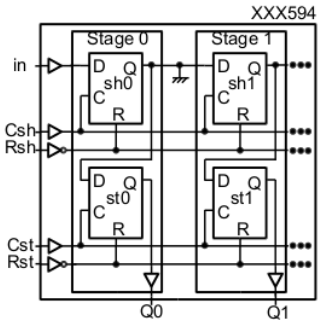


Fig.4. Timing Diagram of the DUT

Furthermore, all components in the testbench are coded by the SystemVerilog. There are classes and a module. The classes are the transaction object, the generator, the interface, the driver, the monitor, the scoreboard, the environment, and the test. However, the testbench top is the module.



(a)



(b)

Fig.5. Stuck-at-faults (a) Stuck-at-1 (b) Stuck-at-0

The transaction object is a base transaction object will be used to verify the DUT may work as the timing diagram shown in Figure 4. Moreover, the base transaction is used in the environment to initiate new transactions and capture transactions at the interface. The code of the transaction object is shown in Figure 6.

```
class Packet;
        bit in;
        bit Csh;
        bit Rsh;
        bit Cst;
        bit Rst;
        rand bit[7:0] Q;
        bit Q7S;
       rand bit[7:0] qsh;
…
endclass
```

Fig.6. Code of the transaction object

The generator is used to generate the random input stimulus signals to be sent to the driver. Figure 7 shows the generator code.

```
class generator;
        int    loop = 10;
        event drv_done;
       mailbox drv_mbx;
….
endclass
```

Fig.7. Code of the generator

Furthermore, the driver is to drive the stimulus signals to the interface and the scoreboard. The code of the driver is shown in Figure 8.

```
class driver;
        virtual switch_if m_switch_vif;
        virtual sh594b_if m_sh594b_vif;
        virtual clk_if  m_clk_vif;
        event drv_done;
       mailbox drv_mbx;
…
endclass
```

Fig.8. Code of the driver

Moreover, the interface contains the stimulus signals driven to the DUT and response signals derived from the DUT. All the signals are required by the DUT to be operated. Figure 9 shows the code of the interface.

```
interface sh594b_if();
        logic in;
        logic Csh;
        logic Rsh;
        logic Cst;
        logic Rst;
        logic[7:0] Q;
        logic Q7S;
        logic[7:0] qsh;
endinterface
```

Fig.9. Code of the driver

Then, the response signals will be monitored by the monitor and captured to the scoreboard. The code of the monitor is shown in Figure 10.

```
class monitor;
        virtual sh594b_if   m_sh594b_vif;
        virtual clk_if     m_clk_vif;
         mailbox scb_mbx;
…
endclass
```

Fig.10. Code of the monitor

Further, the scoreboard will check the response signals compared to expected signals. When the response signals are not match to the expected signals, the DUT is a faulty indicated by *error* statements. Otherwise, pass statements indicate the DUT is a fault-free. Therefore, the scoreboard may have a refence model behaving as the DUT. The reference model code of the scoreboard is shown in Figure 11.

```
class scoreboard;
…
if (!ref_item.Rsh) begin
        {ref_item.qsh} = 0;
    end else begin
        {ref_item.qsh} = {ref_item.qsh[6:0], ref_item.in};
      end
      if (!ref_item.Rst) begin
         {ref_item.Q} = 0;
    end else begin
       {ref_item.Q} = {ref_item.Q[6:0], ref_item.qsh[0]};
    end
…
endclass
```

Fig.11. Reference model of the scoreboard

The environment contains all the verification components, e.g., the generator, driver, interface, the monitor, and the scoreboard. Figure 12 shows the code of the environment.

```
class env;
        generator      g0;
        driver         d0;
        monitor          m0;
        scoreboard       0;
…
endclass
```

Fig.12. Code of the environment

The test contains the environment that can be tweaked with different configuration settings. Also, the test may instantiate any environment. Figure 13 is the code of the test.

```
class test;
        env e0;
       mailbox drv_mbx;
…
endclass
```

Fig.13. Code of the test

The testbench top contains the test. Moreover, the faults are inserted to it by *force* and *release* instructions. The code of the testbench top is shown in Figure 14.

```
module tb_sh594b3sa;
…
sh594b u0 (    .in(in),
               .Csh(Csh),
               .Rsh(Rsh),
               .Cst(Cst),
               .Rst (Rst),
```

```
                .Q(m_sh594b_if.Q),
                .Q7S(m_sh594b_if.Q7S),
               .qsh(qsh));
….
initial begin
test t0;
…
        #35 force qsh[0]=1;
       #4 release qsh[7];
….
endmodule
```

Fig.14. Code of the testbench top

III. RESULTS AND DISCUSSION

Building a testbench is proposed to verify a functionality of a shift register IC from stuck-at-faults. The testbench based on Figure 1 in which the register IC is as a DUT. The DUT is 8-bit shift register produced by Nexperia Co. Ltd in which it has a timing diagram as shown in Figures 4.

The testbench and the DUT are simulated using Questasim simulator. Simulation and transcript results of a fault-free DUT are shown in Figures 15 and 16, respectively. As shown in Figure 15, the result is an identic timing diagram of the DUT in Figure 4. Moreover, the scoreboard indicates *pass* statements verifying the DUT is a fault-free as shown in Figure 7.

In order to verify the DUT from the faults, stucks-at-1 are inserted each output *sh* of stage 0 to stage 7 when the output should be in low level signals. Figures 17 and 18 show simulation and transcript results of faulty DUT, respectively. As shown in Figure 18, error statements in the scoreboard indicate the DUT is a faulty.

```
…
# [11] Scoreboard Pass! Q match ref_item=0x2 item=0x2
# [11] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
…
# [31] Scoreboard Pass! Q match ref_item=0x40 item=0x40
# [31] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
…
# [51] Scoreboard Pass! Q match ref_item=0x0 item=0x0
# [51] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
…
# [71] Scoreboard Pass! Q match ref_item=0x0 item=0x0
# [71] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
….
# [91] Scoreboard Pass! Q match ref_item=0x0 item=0x0
# [91] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
```

Fig.16. Transcript result of fault-free

```
…
# [51] Scoreboard Error! Q mismatch ref_item=0x0 item=0x7
# [51] Scoreboard Pass! Q7S match ref_item=0x0 item=0x0
…
# [71] Scoreboard Error! Q mismatch ref_item=0x0 item=0xff
# [71] Scoreboard Pass! Q7S match ref_item=0x1 item=0x1
…
# [91] Scoreboard Error! Q mismatch ref_item=0x0 item=0xff
# [91] Scoreboard Pass! Q7S match ref_item=0x1 item=0x1
```

Fig.18. Transcript result of faulty DUT

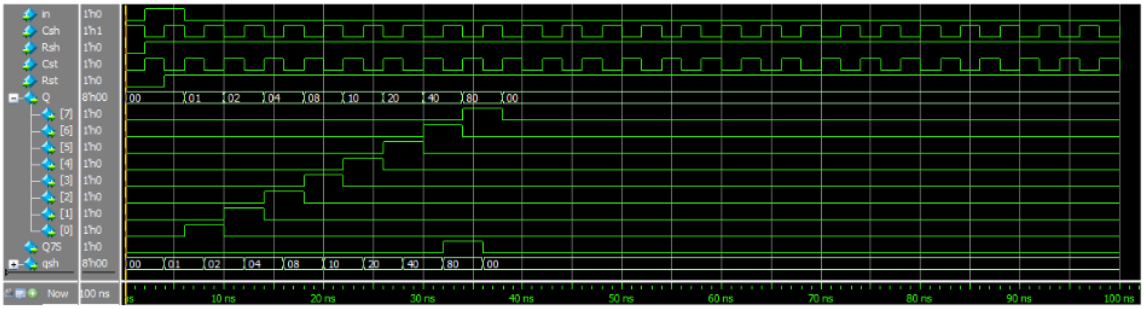


Fig.15. Simulation result of fault-free

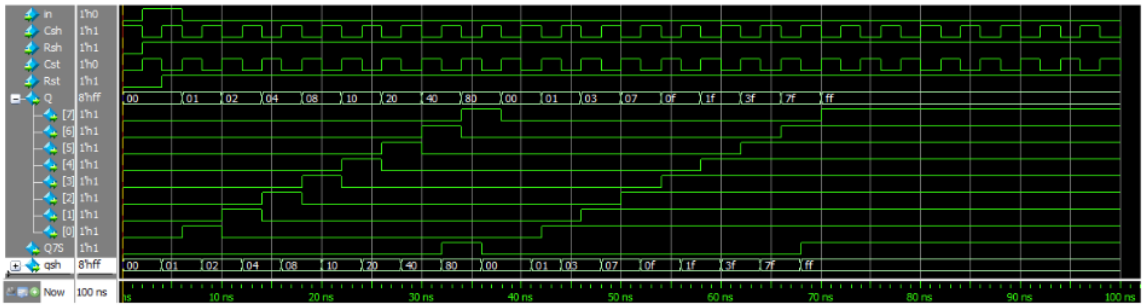


Fig.17. Simulation result of faulty DUT

CONCLUSION

A testbench is built to verify a functionality of a shift register IC by inserting stuck-at-faults inside it. The testbench and the IC are designed by SystemVerilog. Moreover, they are simulated by Questasim simulator. Simulation results show the faults may be detected by the testbench. Moreover, *error* statements will indicate the detected faults in transcript results of the simulator.

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The faults may be detected by an Automatic Test Pattern Generation (ATPG)[6]–[9]. However, it needs to integrate the external tools and programs where integrating them is not easy. Furthermore, it requires a circuit partitioning and a bit parallel processing.

A Built-in Self Test (BIST) was proposed to detect the faults[10]–[12]. The BIST consisted by a signature analyzer[13]. The analyzer is used to compare signals generated by the faults and faults-free and further analyze them. However, it takes time consuming, since the signal faults are detected by checking the generated signals one-by-one. Furthermore, the BIST is still designed by a Verilog Hardware Description Languages (HDL) in which it isn't supported by Object Oriented Programming (OOP) features[14]–[16], thus the detected faults aren't indicated by pass/ error statements.

A SystemVerilog is an extension of the Verilog HDL[17]–[21] used to design and verify hardware[22][23], e.g., Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). The hardware design is created in a Register Transfer Level (RTL) model. Moreover, to verify functionality of the design working as expected, a testbench should be built[24]. The testbench drives different input stimulus to the design and is supported by the OOP features.

In this paper, a proposed shift register IC is designed using the SystemVerilog. It will be verified the functionality from both stuck-at-faults, stuck-at-1 and stuck-at-0 by a testbench. The designed IC and its testbench are simulated using Questasim simulator[25]. Simulation results denote that the faults inside the IC may be detected by the testbench. Furthermore, indicating pass/ error statements is included in the detected faults by it.

II. Research Method

A testbench is built to verify a functionality of a shift register IC from both stuck-at-faults, stuck-at-1 and stuck-at-0. The testbench architecture is shown in Figure 1. There are some supported components, namely, transaction object, generator, interface, driver, monitor, scoreboard, environment, test, and testbench top. The IC is as a Design Under Test (DUT).

Fig.1. Testbench architecture

The DUT is a sample 8-bit shift register IC produced by Nexperia Co. Ltd. A logic diagram of the DUT is shown in Figure 2. As shown in Figure 2, the DUT consists of four buffer gates, two inverter gates, and eight stages, stage 0 to stage 7. Each of the stages is made of a buffer gate and two D flip-flop types in which the D flip-flop types are a shift register *sh* and a storage register *st*. Symbol descriptions in the DUT are shown in Table I.

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First Author and Second Author are with University of Muhammadiyah Malang, Department of Electrical Engineering, Indonesia (e-mail: widianto@umm.ac.id and chasrun@umm.ac.id)

Third Author is with Wroclaw University of Science and Technology, Poland (e-mail: Robert.lis@pwr.edu)