


Artikel 1

Detection of Defective FinFET Logic ICs by Using FFTs

 Widianto

 Publication Articles Jan - Feb 2025 Dosen UMM

 University of Muhammadiyah Malang

Document Details

Submission ID

trn:oid::1:3129761272

Submission Date

Jan 15, 2025, 10:04 AM GMT+7

Download Date

Jan 15, 2025, 10:06 AM GMT+7

File Name

040034_1_5.0192094.pdf

File Size

863.1 KB

6 Pages

2,189 Words

10,519 Characters

17% Overall Similarity

The combined total of all matches, including overlapping sources, for each database.

Filtered from the Report

- Bibliography
- Quoted Text

Exclusions

- 1 Excluded Source

Match Groups

- 19 Not Cited or Quoted 15%**
 Matches with neither in-text citation nor quotation marks
- 4 Missing Quotations 2%**
 Matches that are still very similar to source material
- 0 Missing Citation 0%**
 Matches that have quotation marks, but no in-text citation
- 0 Cited and Quoted 0%**
 Matches with in-text citation present, but no quotation marks

Top Sources

- 15% Internet sources
- 12% Publications
- 4% Submitted works (Student Papers)

Integrity Flags

0 Integrity Flags for Review

No suspicious text manipulations found.

Our system's algorithms look deeply at a document for any inconsistencies that would set it apart from a normal submission. If we notice something strange, we flag it for you to review.

A Flag is not necessarily an indicator of a problem. However, we'd recommend you focus your attention there for further review.

Match Groups

- **19 Not Cited or Quoted 15%**
Matches with neither in-text citation nor quotation marks
- **4 Missing Quotations 2%**
Matches that are still very similar to source material
- **0 Missing Citation 0%**
Matches that have quotation marks, but no in-text citation
- **0 Cited and Quoted 0%**
Matches with in-text citation present, but no quotation marks

Top Sources

- 15% Internet sources
- 12% Publications
- 4% Submitted works (Student Papers)

Top Sources

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

1	Internet		
		eprints.umm.ac.id	10%
2	Student papers		
		University of Muhammadiyah Malang	2%
3	Publication		
		Widianto, Robert Lis. "Delay analysis in HCMOS logic ICs", AIP Publishing, 2022	1%
4	Internet		
		www.frontiersin.org	<1%
5	Student papers		
		University of South Australia	<1%
6	Student papers		
		Universitas Sebelas Maret	<1%
7	Internet		
		apps.dtic.mil	<1%
8	Internet		
		patents.justia.com	<1%
9	Internet		
		ece.uwaterloo.ca	<1%

RESEARCH ARTICLE | MARCH 26 2024

Detection of defective FinFET logic ICs by using FFTs FREE

W. Widiyanto ; Robert Lis; Inda Rusdia Sofiani; La Febry Andira Rose Cynthia



AIP Conf. Proc. 2927, 040034 (2024)

<https://doi.org/10.1063/5.0192094>



APL Energy
Latest Articles Online!
Read Now

Detection of Defective FinFET Logic ICs by Using FFTs

W Widiyanto^{1a)}, Robert Lis²⁾, Inda Rusdia Sofiani¹⁾, La Febry Andira Rose Cynthia¹⁾

¹Department of Electrical Engineering, University of Muhammadiyah Malang, Malang, Indonesia

²Department of Electrical Power Engineering, Wrocław University of Science and Technology, Wrocław, Poland

^{a)}Corresponding author: widiyanto@umm.ac.id

Abstract. A FinFET (Fin Field Effect Transistor) is a non-planar transistor. It has a faster-switching speed, lower power consumption, and static leakage current than CMOSs (Complementary Metal Oxide Semiconductors), which are planar transistors. In the FinFET logic ICs (Integrated Circuits) fabrication process, open defects may occur at interconnects between gates inside them. Open metals may cause defects. Since the FinFET ICs may be operated in high-speed time, the defects are more difficult to analyze in time domain signals. There is a method of FFT (Fast Fourier Transform) computing signals converted from the time domain signals into frequency domain signals. Then, the derived frequency signals will be expressed into the function of the Fourier series. In this paper, the FFT analysis is proposed to detect the defects inside the ICs. The logic ICs of Buffer, AND, and OR are designed by a SPICE (Simulation Program with Integrated Circuit Emphasis) netlist library distributed by Nexperia Co. Ltd. Then, the defects are inserted inside the designed ICs and simulated using LTspice created by Analog Devices Inc. Simulation results show that magnitude signals of defective logic ICs in the Fourier series will decrease linearly with increasing sizes of the defects.

Keywords: FinFET logic ICs, Defective, FFT, SPICE.

INTRODUCTION

Development of ICs (Integrated Circuits) increased very fast. Sizes, performances, power requirements, and package densities are the main parameters of the circuits. Scaling of the circuits may affect improvements in process technology to make them. A FinFET (Fin Field Effect Transistor) technology may be found below 14 nm process nodes [1, 2]. There are some semiconductor foundries that utilized the technology, i.e., TSMC, Intel, Samsung, GlobalFoundries, and others.

The FinFET is a non-planar transistor [3]. It is made of P and N-types, which are composed of source, gate, and drain in each type. A transistor channel of the FinFET is constructed by a thin vertical fin with the gate wrapped fully around the channel and formed between the source and the drain [4]. Thus, the FinFET ICs have lower power consumption, faster-switching speed, and lower static leakage current than CMOS ICs, which are planar transistors.

In the fabrication process of the FinFET ICs, an open defect may occur at interconnect between logic gates inside them [5]. In the layout of the ICs, the defect may be caused by the open metal [6]. Since a metal may form resistance of the interconnects, thus size defects are equal to resistor values.

The open defect between logic gates inside an IC was detected by IDDQ testing [7]. Moreover, delay testing was proposed to detect the open defects [8, 9]. However, the defective ICs were still tested in time domain signals. Since the FinFET ICs may be operated at a high-speed time, so they are more difficult to be analyzed.

In order to simplify the signals analysis, they were evaluated in frequency domain signals by using FFTs [10]. The FFT may convert the signals from the time domains to the frequency domains and vice versa [11]. Thus, the FFT may be applicable to analyze signals generated by the FinFET ICs.

In this paper, the FFT analysis is proposed to detect the defects inside the ICs. The ICs are designed by a SPICE (Simulation Program with Integrated Circuit Emphasis) [12] netlist library distributed by Nexperia Co. Ltd [13].

Then, they are simulated using LTspice created by Analog Devices Inc. Simulation results show that magnitude signals of defective ICs will decrease linearly with increasing sizes of the defects.

METHODS

In a FinFET logic IC, it consists of a logic diagram by input voltages V_{i1} to V_{in} and output voltages V_{o1} to V_{on} . This is shown in **FIGURE 1**. The diagram makes different specific functions of the IC, for example, Buffer, OR, and AND. Moreover, the diagram is composed of some logic gates.

Open defects may occur at interconnects between logic gates inside the IC. The defective IC may be analyzed by measuring the signal generated by it in the output voltages. However, the common generated signals are domain time signals. In order to simplify the defects analysis, the domain time signals should be converted to domain frequency signals.

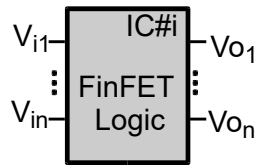


FIGURE 1. Logic Diagram of FinFET IC

An FFT is a method to compute signals converted from time domain signals into frequency domain signals. Then, the derived frequency signals will be expressed into the function of the Fourier series. There are common types of signal waveforms converted by the FFT, i.e., triangular, square, parabola, and full wave rectified sine.

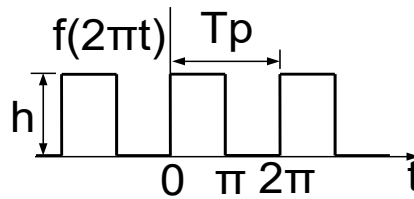


FIGURE 2. Signal Square Waveform

For example, the signal square waveform is illustrated in **FIGURE 2**. The waveform is defined in **Equation 1**. A fundamental frequency of the waveform is defined by **Equation 2**. The waveform is defined by the function of the Fourier series as denoted in **Equation 3**. However, the magnitude of the series will decay slowly as $1/n$, where n is the number of points.

$$f(2\pi t) = h \text{ for } 0 \leq 2\pi t \leq \pi \text{ and } f(x) = 0 \text{ for } \pi \leq 2\pi t \leq 2\pi \tag{1}$$

$$f_0 = \frac{1}{T_p} \tag{2}$$

$$f(2\pi t) = \frac{h}{2} + \frac{2h}{\pi} \left[\sin(2\pi t) + \frac{1}{3} \sin(6\pi t) + \frac{1}{5} \sin(10\pi t) + \frac{1}{7} \sin(14\pi t) + \dots \right] \tag{3}$$

RESULTS AND DISCUSSION

In order to analyze FFTs in defective FinFET logic ICs, therefore Buffer, OR, and AND IC designs are proposed. They are designed by a SPICE netlist library distributed by Nexperia Co. Ltd. Moreover, they are simulated using the free SPICE simulator of LTspice created by Analog Devices.

The defective FinFET IC designs are shown in **FIGURE 3**. The Buffer IC has three targeted open defects at interconnects between composed gates, i.e., *a*, *b*, and *c* nodes. Moreover, the OR and the AND ICs have three targeted defects located at the *a*, *b*, *c*, and *f* nodes. Resistors of 100 Ω, 1 kΩ, 1 MΩ, and 1 TΩ are inserted into the targeted defects.

A square waveform signal is provided to an input voltage V_i . As the waveform illustrated in **FIGURE 2**, an amplitude h and a time period T_p of V_i are 3 V and 2 μs, respectively. V_{DD} and GND are 3 V and 0 V, respectively. After inserting the resistor into the targeted defects, a generated signal of the ICs is measured in an output voltage V_o . The generated signal will be analyzed by using the FFT, which is facilitated by the LTspice.

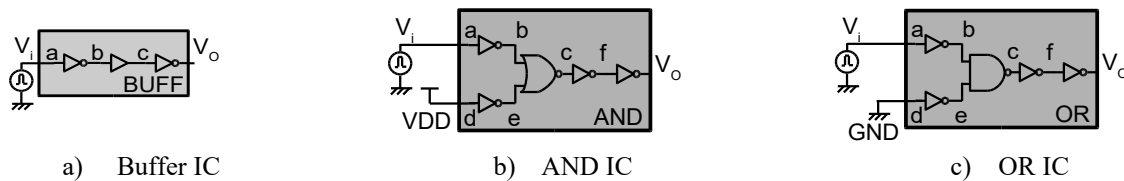


FIGURE 3. FinFET logic IC Designs

The FFT signal result of the defective Buffer IC by inserting the resistors of 100 Ω, 1 kΩ, and 1 MΩ to the targeted defects is shown in **FIGURE 4**. The result is represented by a function of the Fourier series as defined in Equation 3. Moreover, a fundamental frequency of the result is defined as Equation 2.

Furthermore, the FFT signal results of the defective Buffer, the NOR, and the AND ICs are charted in **FIGURES 5, 6, and 7**, respectively. As shown in **FIGURES 5a, 6a, and 7a**, the magnitudes of the function will decrease linearly with increasing the inserted resistor values.

Compared to delay testing results of open defects occurring at interconnects between gates inside ICs, the testing is derived from low-speed responses of the ICs in time domain signals[9]. Since measuring the delays is not facilitated by the LTspice, not like the FFT; thus the testing is not easy to analyze in high-speed responses.

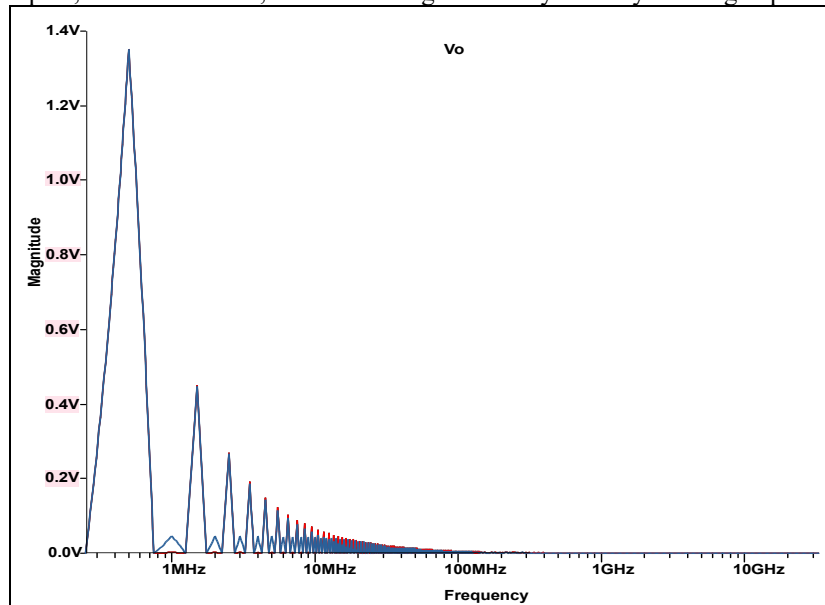


FIGURE 4. FFT Result of Buffer FinFET IC

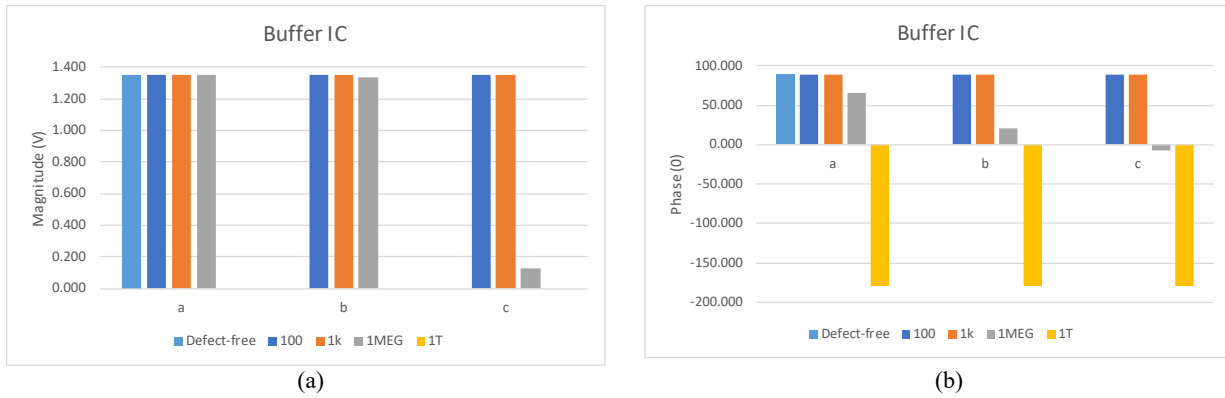


FIGURE 5. (a) The magnitude of Buffer IC and (b) The phase of Buffer IC

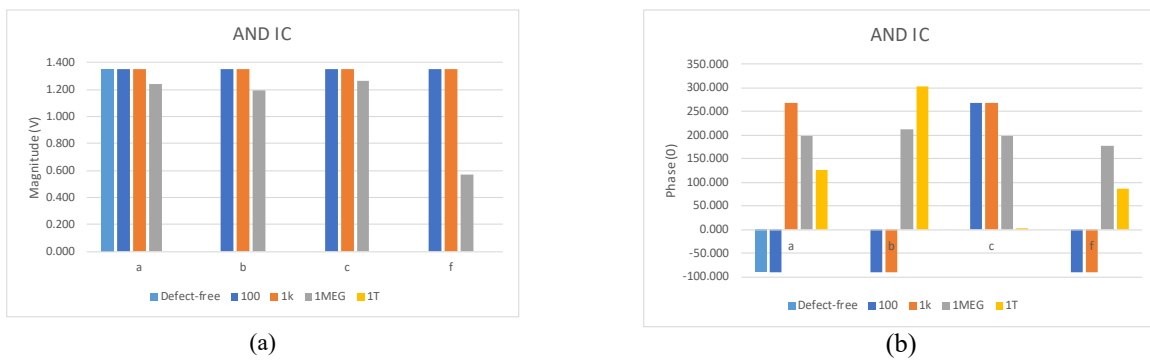


FIGURE 6. (a) The magnitude of AND IC and (b) The phase of AND IC

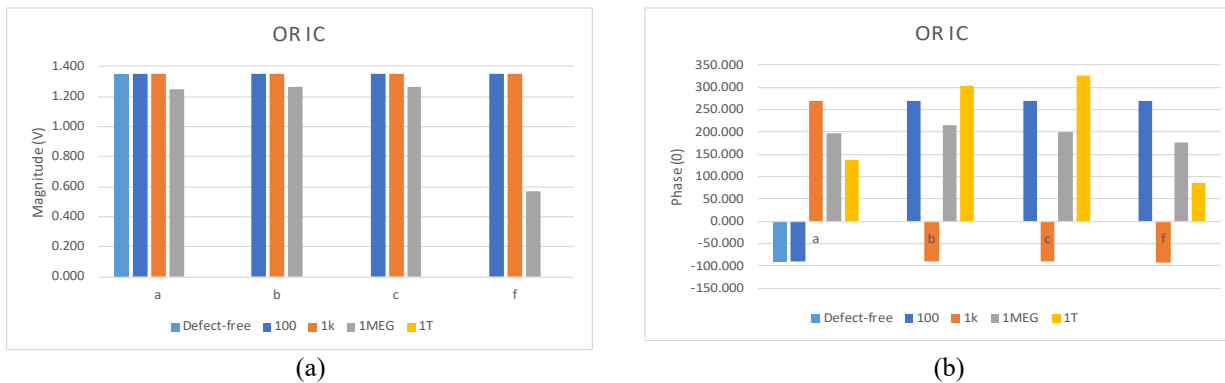


FIGURE 7. The magnitude of OR IC and (b) The phase of OR IC

CONCLUSIONS

An FFT was proposed to analyze defective FinFET logic ICs caused by open defects occurring at interconnects between composed logic gates inside them. The proposed defective ICs are Buffer, AND, and OR ICs. The open defects are targeted by inserting resistors of 100 Ω – 1 TΩ into the interconnects. The FFT results of the defective ICs will generate a function of the Fourier series. However, the magnitudes of the function will decrease linearly with increasing the inserted resistors.

REFERENCES

- [1] N. E. I. Boukourt, T. R. Lenka, S. Patanè, and G. Crupi, "Effects of Varying the Fin Width, Fin Height, Gate Dielectric Material, and Gate Length on the DC and RF Performance of a 14-nm SOI FinFET Structure," *Electronics*, vol. 11, no. 1, 2022.
- [2] P. Oldiges *et al.*, "Chip Power-Frequency Scaling in 10/7nm Node," *IEEE Access*, vol. 8, pp. 154329-154337, 2020.
- [3] S. K. Saha, *FinFET devices for VLSI circuits and systems*. CRC Press, 2020.
- [4] S. Kim *et al.*, "Investigation of Device Performance for Fin Angle Optimization in FinFET and Gate-All-Around FETs for 3 nm-Node and Beyond," *IEEE Transactions on Electron Devices*, vol. 69, no. 4, pp. 2088-2093, 2022.
- [5] Y. Hashim, "The impact of channel fin width on electrical characteristics of Si-FinFET," *International Journal of Electrical and Computer Engineering*, vol. 12, no. 1, 2022.
- [6] F. Forero, J. M. Galliere, M. Renovell, and V. Champac, "A Semi-analytical Model for Interconnect Open Defects in FinFET Logic Cells," in *2019 IEEE Latin American Test Symposium (LATS)*, 2019, pp. 1-6.
- [7] J. Y. Liao, S. Rahimi, C. Schmidt, and H. L. Marks, "Failure Analysis of Total-Dose Radiation-Induced Degradation on FinFET Logic ICs," pp. 341-344: ASM International.
- [8] F. Forero, H. Villacorta, M. Renovell, and V. Champac, "Modeling and Detectability of Full Open Gate Defects in FinFET Technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 9, pp. 2180-2190, 2019.
- [9] Widiyanto and R. Lis, "Delay analysis in HCMOS logic ICs," *AIP Conference Proceedings*, vol. 2453, no. 1, p. 020059, 2022/07/25 2022, DOI: <https://doi.org/10.1063/5.0094353>.
- [10] S. Bailey *et al.*, "A Mixed-Signal RISC-V Signal Analysis SoC Generator With a 16-nm FinFET Instance," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 10, pp. 2786-2801, 2019.
- [11] Z. X. B. A. I. Y. C. X. Z. Y. Ma Liping, "An Accuracy Dynamically Configurable FFT Processor Based on Approximate Computing," *Journal of Shanghai Jiaotong University*, vol. 56, no. 2, pp. 223-230, 2022.
- [12] A. U. H. Pampori, S. A. Ahsan, and Y. S. Chauhan, "Modeling the Impact of Dynamic Fin-Width on the I ; V , C ; V and RF Characteristics of GaN Fin-HEMTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 5, pp. 2275-2281, 2022.
- [13] M. Sarkar, S. T. Nasir, I. Chakraborty, S. Maity, R. Chakraborty, and G. S. Taki, "Performance Analysis of Various FINFET Threshold Logic based Full Adder Design," in *2019 3rd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech)*, 2019, pp. 1-5.



Digital Receipt

This receipt acknowledges that Turnitin received your paper. Below you will find the receipt information regarding your submission.

The first page of your submissions is displayed below.

Submission author: Artikel 1
Assignment title: Widianto
Submission title: Detection of Defective FinFET Logic ICs by Using FFTs
File name: 040034_1_5.0192094.pdf
File size: 863.09K
Page count: 6
Word count: 2,189
Character count: 10,519
Submission date: 15-Jan-2025 10:05AM (UTC+0700)
Submission ID: 2564404330

