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Detection of Defective FinFET Logic ICs by Using FFTs

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Abstract. A FinFET (Fin Field Effect Transistor) is a non-planar transistor. It has a faster-switching speed, lower power consumption, and static leakage current than CMOSs (Complementary Metal Oxide Semiconductors), which are planar transistors. In the FinFET logic ICs (Integrated Circuits) fabrication process, open defects may occur at interconnects between gates inside them. Open metals may cause defects. Since the FinFET ICs may be operated in high-speed time, the defects are more difficult to analyze in time domain signals. There is a method of FFT (Fast Fourier Transform) computing signals converted from the time domain signals into frequency domain signals. Then, the derived frequency signals will be expressed into the function of the Fourier series. In this paper, the FFT analysis is proposed to detect the defects inside the ICs. The logic ICs of Buffer, AND, and OR are designed by a SPICE (Simulation Program with Integrated Circuit Emphasis) netlist library distributed by Nexperia Co. Ltd. Then, the defects are inserted inside the designed ICs and simulated using LTspice created by Analog Devices Inc. Simulation results show that magnitude signals of defective logic ICs in the Fourier series will decrease linearly with increasing sizes of the defects.

Keywords: FinFET logic ICs, Defective, FFT, SPICE.

INTRODUCTION

Development of ICs (Integrated Circuits) increased very fast. Sizes, performances, power requirements, and package densities are the main parameters of the circuits. Scaling of the circuits may affect improvements in process technology to make them. A FinFET (Fin Field Effect Transistor) technology may be found below 14 nm process nodes [1, 2]. There are some semiconductor foundries that utilized the technology, i.e., TSMC, Intel, Samsung, GlobalFoundires, and others.

The FinFET is a non-planar transistor [3]. It is made of P and N-types, which are composed of source, gate, and drain in each type. A transistor channel of the FinFET is constructed by a thin vertical fin with the gate wrapped fully around the channel and formed between the source and the drain [4]. Thus, the FinFET ICs have lower power consumption, faster-switching speed, and lower static leakage current than CMOS ICs, which are planar transistors.

In the fabrication process of the FinFET ICs, an open defect may occur at interconnect between logic gates inside them [5]. In the layout of the ICs, the defect may be caused by the open metal [6]. Since a metal may form resistance of the interconnects, thus size defects are equal to resistor values.

The open defect between logic gates inside an IC was detected by IDDQ testing [7]. Moreover, delay testing was proposed to detect the open defects [8, 9]. However, the defective ICs were still tested in time domain signals. Since the FinFET ICs may be operated at a high-speed time, so they are more difficult to be analyzed.

In order to simplify the signals analysis, they were evaluated in frequency domain signals by using FFTs [10]. The FFT may convert the signals from the time domains to the frequency domains and vice versa [11]. Thus, the FFT may be applicable to analyze signals generated by the FinFET ICs.

In this paper, the FFT analysis is proposed to detect the defects inside the ICs. The ICs are designed by a SPICE (Simulation Program with Integrated Circuit Emphasis) [12] netlist library distributed by Nexperia Co. Ltd [13].

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Then, they are simulated using LTspice created by Analog Devices Inc. Simulation results show that magnitude signals of defective ICs will decrease linearly with increasing sizes of the defects.

METHODS

In a FinFET logic IC, it consists of a logic diagram by input voltages *Vi*1 to *Vi*n and output voltages *Vo*1 to *Vo*n. This is shown in **FIGURE 1**. The diagram makes different specific functions of the IC, for example, Buffer, OR, and AND. Moreover, the diagram is composed of some logic gates.

Open defects may occur at interconnects between logic gates inside the IC. The defective IC may be analyzed by measuring the signal generated by it in the output voltages. However, the common generated signals are domain time signals. In order to simplify the defects analysis, the domain time signals should be converted to domain frequency signals.

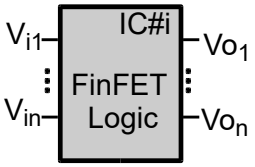


FIGURE 1. Logic Diagram of FinFET IC

An FFT is a method to compute signals converted from time domain signals into frequency domain signals. Then, the derived frequency signals will be expressed into the function of the Fourier series. There are common types of signal waveforms converted by the FFT, i.e., triangular, square, parabola, and full wave rectified sine.

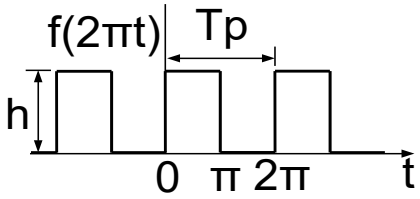


FIGURE 2. Signal Square Waveform

For example, the signal square waveform is illustrated in **FIGURE 2**. The waveform is defined in **Equation 1**. A fundamental frequency of the waveform is defined by **Equation 2**. The waveform is defined by the function of the Fourier series as denoted in **Equation 3**. However, the magnitude of the series will decay slowly as 1/n, where n is the number of points.

$$f(2\pi t) = h \text{ for } 0 \le 2\pi t \le \pi \text{ and } f(x) = 0 \text{ for } \pi \le 2\pi t \le 2\pi \quad (1)$$

$$f0 = \frac{1}{Tp} \quad (2)$$

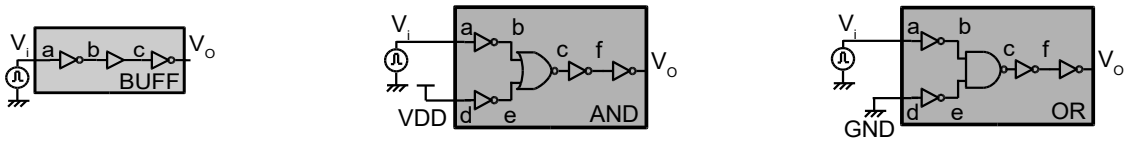
$$f(2\pi t) = \frac{h}{2} + \frac{2h}{\pi}\left[\sin(2\pi t) + \frac{1}{3}\sin(6\pi t) + \frac{1}{5}\sin(10\pi t) + \frac{1}{7}\sin(14\pi t) + \cdots\right] \quad (3)$$

RESULTS AND DISCUSSION

In order to analyze FFTs in defective FinFET logic ICs, therefore Buffer, OR, and AND IC designs are proposed. They are designed by a SPICE netlist library distributed by Nexperia Co. Ltd. Moreover, they are simulated using the free SPICE simulator of LTspice created by Analog Devices.

The defective FinFET IC designs are shown in **FIGURE 3**. The Buffer IC has three targeted open defects at interconnects between composed gates, i.e., *a*, *b*, and *c* nodes. Moreover, the OR and the AND ICs have three targeted defects located at the *a*, *b*, *c*, and *f* nodes. Resistors of 100 Ω, 1 kΩ, 1 MΩ, and 1 TΩ are inserted into the targeted defects.

A square waveform signal is provided to an input voltage *Vi*. As the waveform illustrated in **FIGURE 2**, an amplitude *h* and a time period *Tp* of *Vi* are 3 V and 2 µs, respectively. *VDD* and *GND* are 3 V and 0 V, respectively. After inserting the resistor into the targeted defects, a generated signal of the ICs is measured in an output voltage *Vo*. The generated signal will be analyzed by using the FFT, which is facilitated by the LTspice.



a) Buffer IC b) AND IC c) OR IC

FIGURE 3. FinFET logic IC Designs

The FFT signal result of the defective Buffer IC by inserting the resistors of 100 Ω, 1 kΩ, and 1 MΩ to the targeted defects is shown in **FIGURE 4**. The result is represented by a function of the Fourier series as defined in Equation 3. Moreover, a fundamental frequency of the result is defined as Equation 2.

Furthermore, the FFT signal results of the defective Buffer, the NOR, and the AND ICs are charted in **FIGURES 5, 6,** and **7**, respectively. As shown in **FIGURES 5a, 6a,** and **7a**, the magnitudes of the function will decrease linearly with increasing the inserted resistor values.

Compared to delay testing results of open defects occurring at interconnects between gates inside ICs, the testing is derived from low-speed responses of the ICs in time domain signals[9]. Since measuring the delays is not facilitated by the LTspice, not like the FFT; thus the testing is not easy to analyze in high-speed responses.

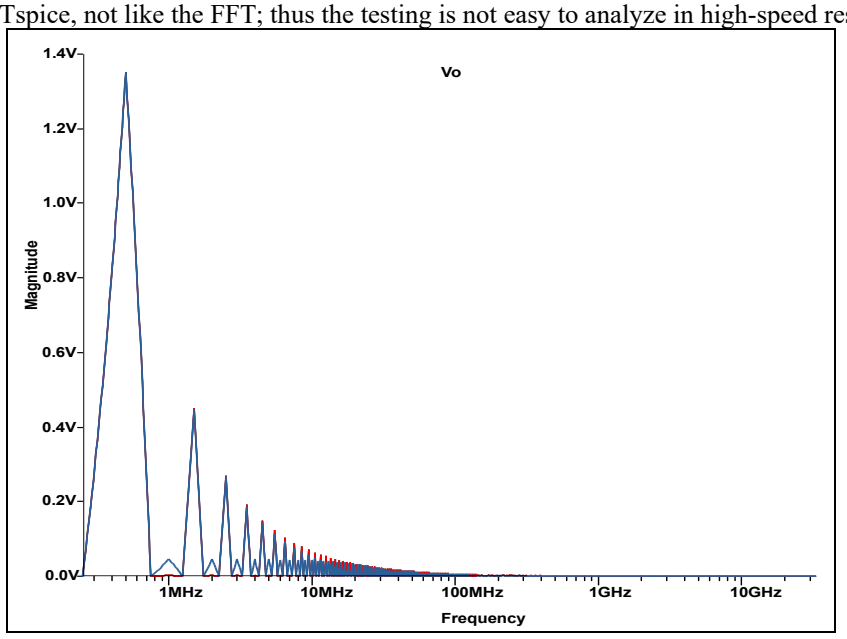
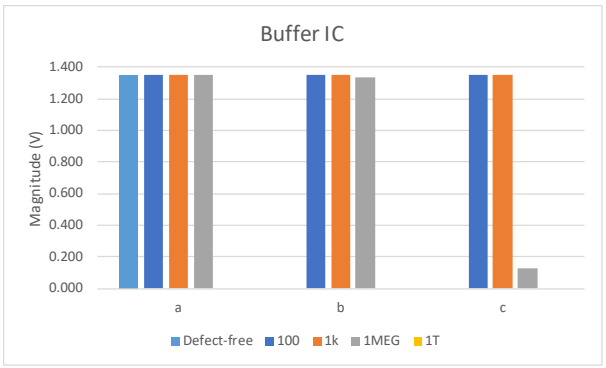
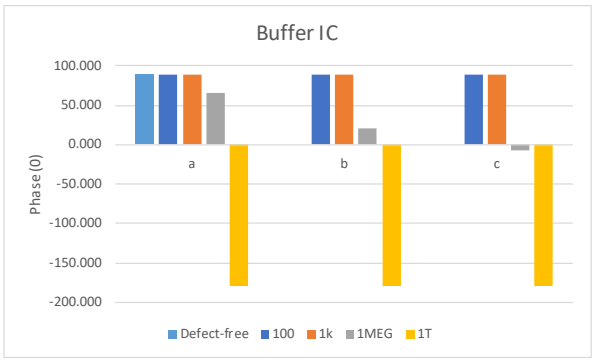


FIGURE 4. FFT Result of Buffer FinFET IC

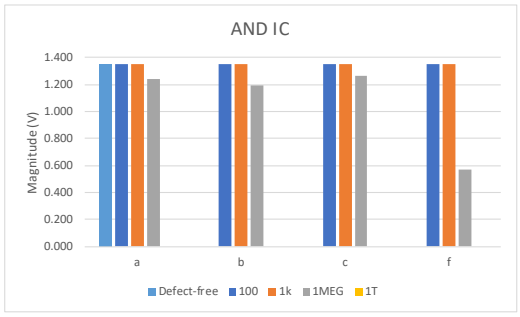


(a)

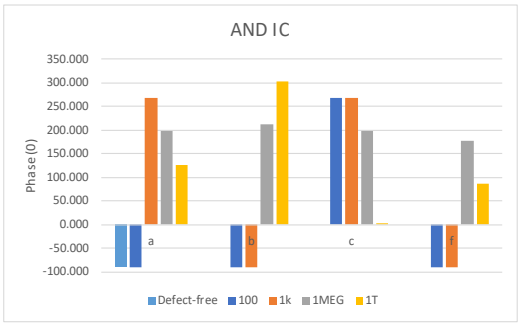


(b)

FIGURE 5. (a) The magnitude of Buffer IC and (b) The phase of Buffer IC

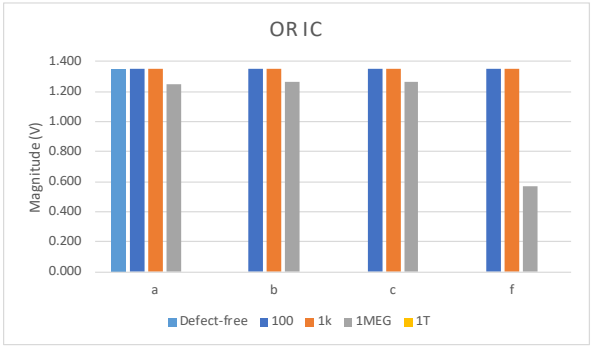


(a)

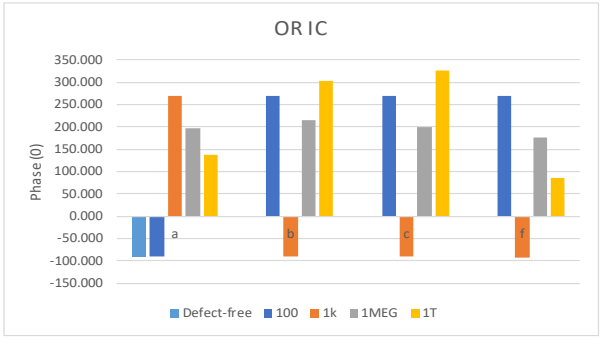


(b)

FIGURE 6. (a) The magnitude of AND IC and (b) The phase of AND IC



(a)



(b)

FIGURE 7. The magnitude of OR IC and (b) The phase of OR IC

CONCLUSIONS

An FFT was proposed to analyze defective FinFET logic ICs caused by open defects occurring at interconnects between composed logic gates inside them. The proposed defective ICs are Buffer, AND, and OR ICs. The open defects are targeted by inserting resistors of 100 Ω – 1 TΩ into the interconnects. The FFT results of the defective ICs will generate a function of the Fourier series. However, the magnitudes of the function will decrease linearly with increasing the inserted resistors.

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