BAB IV

Widianto Syafaah HCMOS Testing Defect

Suhardi Syafaah Irfan - MPPT Improvement photovolataic solar panel GWO
Teknik Elektro
University of Muhammadiyah Malang

Document Details

Submission ID
trn:oid:::1:2999754889

Submission Date
Sep 6, 2024, 1:45 PM GMT+7

Download Date
Sep 6, 2024, 1:46 PM GMT+7

File Name
urhadi_-_IDDQ_Testing_Resistive_Detection_Open_Deffect_HCMOS.pdf

File Size
210.5 KB

3 Pages

1,271 Words

5,821 Characters

19% Overall Similarity

The combined total of all matches, including overlapping sources, for each database.

Filtered from the Report

- Bibliography
- Quoted Text

Exclusions

- 6 Excluded Sources

Match Groups

21 Not Cited or Quoted 19%
Matches with neither in-text citation nor quotation marks

0 Missing Quotations 0%
Matches that are still very similar to source material

0 Missing Citation 0%
Matches that have quotation marks, but no in-text citation

0 Cited and Quoted 0%
Matches with in-text citation present, but no quotation marks

Top Sources

4% Internet sources
18% Publications
9% Submitted works (Student Papers)

Integrity Flags

1 Integrity Flag for Review

Hidden Text
0 suspect characters on 3 pages
Text is altered to blend into the white background of the document.

Our system's algorithms look deeply at a document for any inconsistencies that would set it apart from a normal submission. If we notice something strange, we flag it for you to review.

A Flag is not necessarily an indicator of a problem. However, we'd recommend you focus your attention there for further review.

Match Groups

- **21** Not Cited or Quoted 19%
  Matches with neither in-text citation nor quotation marks
- **0** Missing Quotations 0%
  Matches that are still very similar to source material
- **0** Missing Citation 0%
  Matches that have quotation marks, but no in-text citation
- **0** Cited and Quoted 0%
  Matches with in-text citation present, but no quotation marks

Top Sources

- 4% Internet sources
- 18% Publications
- 9% Submitted works (Student Papers)

Top Sources

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

1	Publication	
Widianto, Robert Lis. "Delay analysis in HCMOS logic ICs", AIP Publishing, 2022		4%
2	Student papers	
Universiti Teknikal Malaysia Melaka		3%
3	Publication	
Takumi Miyabe, Masaki Hashizume, Hiroyuki Yotsuyanagi, Shyue-Kung Lu, Zvi Ro...		3%
4	Student papers	
Universitas Islam Indonesia		3%
5	Publication	
Tomoaki Konishi, Hiroyuki Yotsuyanagi, Masaki Hashizume. "A built-in test circuit...		2%
6	Publication	
Hashizume, Masaki, Shoichi Umezu, Hiroyuki Yotsuyanagi, and Shyue-Kung Lu. "...		2%
7	Publication	
Widianto, , Hiroyuki Yotsuyanagi, Akira Ono, Masao Takagi, Zvi Roth, and Masaki ...		2%

Seminar Nasional Teknologi dan Rekayasa (SENTRA) 2017
ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

IDDQ TESTING FOR DETECTING RESISTIVE OPEN DEFECTS IN HCMOS LOGIC ICS

Widianto*[1], Lailis Syafaah[2], Nurhadi[3]
[1,2,3]University of Muhammadiyah Malang

Kontak person:
Widianto
e-mail: widianto@umm.ac.id[1]

Abstract

Resistive open defects may occur at an input gate in a HCMOS logic IC. The defects may be caused by an opened metal line and may degrade performances of the IC. An IDDQ testing is proposed to detect the defects. The testing is based on measuring a quiescent supply current IDDQ value which flows to the IC. The defective IC is detected by flowing the larger IDDQ value compared to the defect-free IC. Feasibility of the testing is implemented in the IC designed by a SPICE library of NXP semiconductor Co. Ltd and is examined using a SPICE simulation of LTSpiceIV. Simulation results show that the resistive open defects may be detected by the IDDQ testing.

Keywords: *resistive open defects, HCMOS IC, IDDQ testing, defective IC*

1. Introduction

In an IC (integrated circuits) technology related to Moore law's, a speed of ICs will increase doubled roughly every 34 months[1]. A mentioned phenomenon may occur in CMOS (complementary metal oxide semiconductor) ICs which develop to HCMOS (high speed CMOS) ICs. However, open defects may occur inside the CMOS ICs as well as the HCMOS ICs by opened input gates[2]. Thus, the defects should be tested before shipping the HCMOS ICs to be delivered to customers.

The open defects are opens at metal lines. They are caused by the increasing number contacts and vias[3]. The open defects may differentiate into two parts, i.e. a hard open defect and a resistive open defect. The hard open defect disconnects fully the metal lines. On the other hand, the metal lines are disconnected partially by the resistive open defect.

The hard open defect inside the ICs can be detected by an I_{DDQ} testing based measuring its quiescent supply current[4]. The quiescent supply current IDDQ of the ICs by the open defect will be larger compared to defect-free ICs. However, test input vectors should be determined earlier to detect the defect.

An IDDQ testing regardless generated test input vectors was proposed to detect the hard open defect[5]. A DUT of the IC was made to evaluate feasibility of the testing in detecting the defect. However, in the proposed DUT, the resistive open defect may not be detected by the testing. Thus, the DUT of the IC should be revised in order to detect the resistive open defect by the testing.

In this paper, an IDDQ testing by a new DUT is proposed to detect the resistive open defect. In order to evaluate feasibility of the testing in detecting the resistive open defect, the DUT is examined using a SPICE simulation of LTSpiceIV. The DUT is made by a SPICE netlist library distributed by NXP Co. Ltd. Furthermore, analysis results are denoted in this paper.

2. Research Method

An IDDQ testing is proposed to detect resistive open defects in a HCMOS IC. The testable DUT (device under test) IC is shown in Figure 1. The IC consists of input pins I1 to In, output pins O1 to On, and a supply voltage pin VDD. Furthermore, it is made of protection circuits, inverters, and a logic core. The logic core may be inverter, NAND, NOR, and other logic gates. A targeted resistive open defect is denoted as "*a*" in the IC. The IDDQ testing may detect the targeted defect by measuring a quiescent supply current IDDQ of the IC.

For an example, an inverter gate is used as the logic core. Electrical characteristics of the inverter gate are shown in Fig. 2. As shown in Fig. 2(b), when an input voltage of the gate *Vi* is a *H* or a *L* level, supply current iDD of almost zero will flow into the gate. On the other hand, if *Vi* is in a range specified by Eq. (1), large iDD will flow, since both a pMOS P_1 and an nMOS N_1 in the gate turn on.

When a resistive open defect occurs at the targeted *a*, a large quiescent supply current IDDQ flows to the IC, regardless either a *H* or a *L* level signal is provided to an input pin of the IC I_1, since the input voltage of the inverter as the logic core is the range specified by Eq. (1). However, in the defect-

ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

free IC, the IDDQ is almost zero will flow to the IC, when the input voltage of the inverter is either a *H* or a *L* level signal.

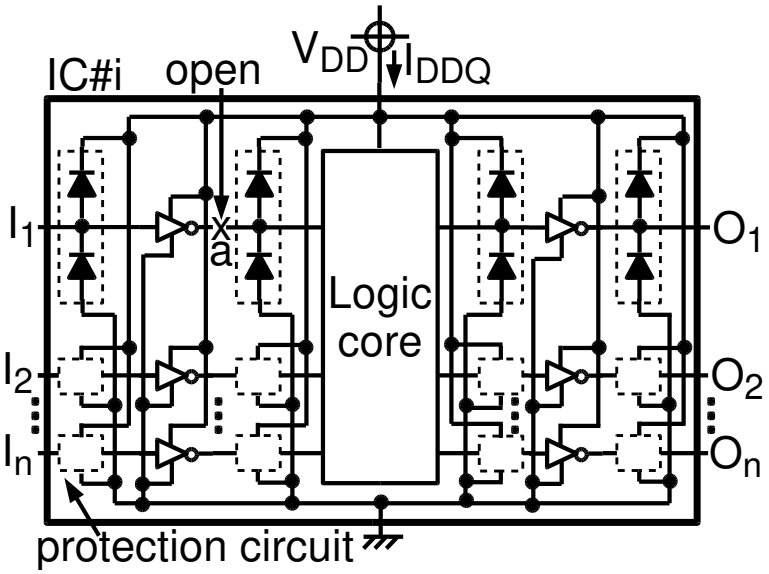
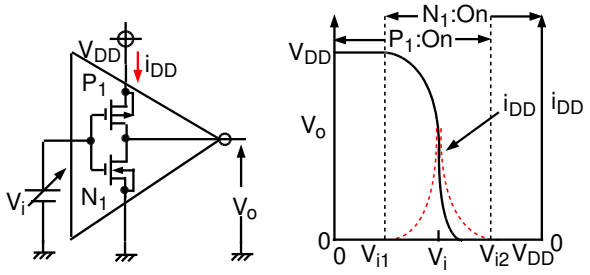


Figure 1. DUT IC

$$Vi_1 \le Vi \le Vi_2 \quad (1)$$



(a)Measurement circuit (b) DC characteristics

Figure 2. Electrical characteristics of inverter gate

3. Results and Discussion

In order to evaluate feasibility of an IDDQ testing in detecting a resistive open defect which occurs at an input gate of a HCMOS IC, a simulation circuit is made as shown in Figure 3. Two ICs, IC#1 and IC#2, are implemented in the circuit. A SPICE netlist library of NXP Co. Ltd is used to design both the ICs. IC#2 is a DUT which denoted "*a*" as a targeted resistive open defect.

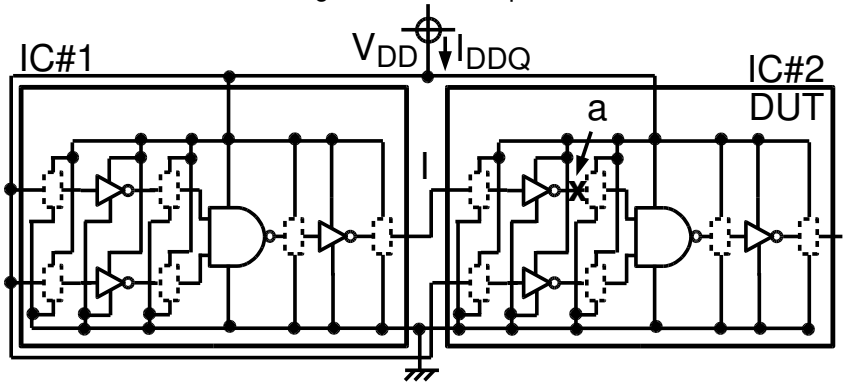
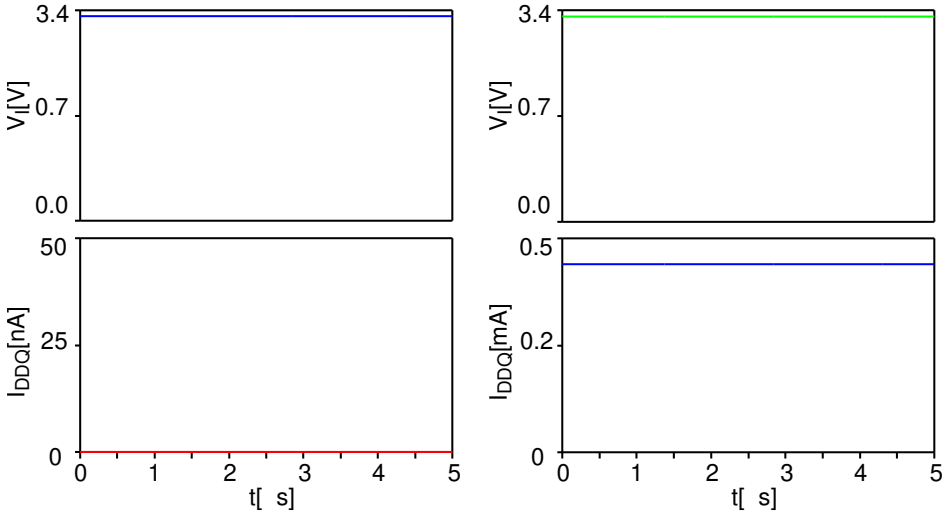


Figure 3. Simulation circuit

ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

A supply voltage VDD and *a* are provided by 3.3 V and a resistor 100 G , respectively. Moreover, the circuit is simulated using a SPICE simulation of LTSpiceIV. It is tested using the IDDQ testing by measuring a quiescent supply current IDDQ. Simulation results are shown in Figure 4. In defect-free ICs, the IDDQ is almost zero flows to the circuit as shown in Figure 4(a). In Figure 4(b), the defective circuit caused by the resistive open defect in the targeted *a is* detected by flowing the large IDDQ.



(a) Defect-free ICs (b) Resistive open one

Figure 4. Simulation results

4. Conclusion

A resistive open defect occurring in an input gate of a HCMOS IC may be detected using an IDDQ testing. The testing is based on measuring a quiescent supply current IDDQ of the IC. The resistive open defect is detected by flowing the larger IDDQ compared to the defect-free IC. In order to locate the defect, it is a future work.

Acknowledgment

This work was supported by grant PUSKAREKATEK 2017 from Faculty of Engineering, Universsity of Muhammadiyah Malang.

References

[1] Neil HEW, David MH. CMOS VLSI Design. A Circuits and Systems Perspective. Fourth Edition. Addison Wesley. 2011
[2] Grout IA. Integrated Circuit Test Engineering. Springer. 2006.
[3] Kruseman et. al. *Comparison of IDDQ testing and Very-Low Voltage Testing*. Proceeding of International Test Conference. 2002: 964 - 973.
[4] Pathirana RMPW. Effective IDDQ Testing Method to Identify The Fault in Low Voltage CMOS Circuits.
[5] Widianto et. al. *Open Defect Detection of CMOS ICs by Using IDDQ Testing*. Proceeding SENTRA. 2016: 169 - 173