BAB 1

Widianto Syafaah CMOS

Irfan Syafaah Ariyanto Faruq - permanent magnet generator turbine energy
Teknik Elektro
University of Muhammadiyah Malang

Document Details

Submission ID
trn:oid:::1:2999639257

Submission Date
Sep 6, 2024, 10:57 AM GMT+7

Download Date
Sep 6, 2024, 10:59 AM GMT+7

File Name
ianto_Syafaah_Nurhadi_-_SELF_TEST_DETECTING_STUCK-AT_CMOS_IC.pdf

File Size
186.5 KB

4 Pages

1,420 Words

6,329 Characters

8% Overall Similarity

The combined total of all matches, including overlapping sources, for each database.

Filtered from the Report

- Bibliography
- Quoted Text

Exclusions

- 2 Excluded Sources

Match Groups

8 Not Cited or Quoted 6%
Matches with neither in-text citation nor quotation marks

0 Missing Quotations 0%
Matches that are still very similar to source material

0 Missing Citation 0%
Matches that have quotation marks, but no in-text citation

0 Cited and Quoted 0%
Matches with in-text citation present, but no quotation marks

Top Sources

0% Internet sources
4% Publications
4% Submitted works (Student Papers)

Integrity Flags

1 Integrity Flag for Review

Hidden Text
0 suspect characters on 2 pages
Text is altered to blend into the white background of the document.

Our system's algorithms look deeply at a document for any inconsistencies that would set it apart from a normal submission. If we notice something strange, we flag it for you to review.

A Flag is not necessarily an indicator of a problem. However, we'd recommend you focus your attention there for further review.

Match Groups

- **8** Not Cited or Quoted 6%
  Matches with neither in-text citation nor quotation marks
- **0** Missing Quotations 0%
  Matches that are still very similar to source material
- **0** Missing Citation 0%
  Matches that have quotation marks, but no in-text citation
- **0** Cited and Quoted 0%
  Matches with in-text citation present, but no quotation marks

Top Sources

0% Internet sources
4% Publications
4% Submitted works (Student Papers)

Top Sources

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

1 Student papers
Universitas Islam Lamongan 4%

2 Publication
Daniel P. Siewiorek, Robert S. Swarz. "Reliable Computer Systems - Design and Ev... 2%

3 Publication
Svetlana N. Yanushkevich, Vlad P. Shmerko. "Introduction to Logic Design", CRC P... 2%

Seminar Nasional Teknologi dan Rekayasa (SENTRA) 2018
ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

BUILT-IN SELF TEST FOR DETECTING STUCK-AT-FAULTS IN CMOS COMBINATIONAL LOGIC ICS

Widianto[*1], Lailis Syafaah[2], Nurhadi[3]
Teknik Elektro/Universitas Muhammadiyah Malang

Contact Person:
Widianto
Raya Tlogomas 246 Malang, Telp/Fax 0341-464318 ext 129
E-mail: widianto@umm.ac.id

Abstract

Stuck-at-faults may occur at input and output gates inside CMOS combinational logic ICs. The faults may be caused by an imperfect manufacturing process. Moreover, they may generate a function of the ICs becomes errors. There are two types of the faults, namely stuck-at-1 and stuck-at-0. The stuck-at-1 and the stuck-at-0 may affect logic values of the gates become 1 and 0, respectively. Thus, they should be detected early. In this paper, a built-in self test circuit is proposed to detect them. The test circuit consists of a linear feedback shift register and multiplexers. The shift register is made by D-flip flops and an XOR gate and is used to generate test vectors. The multiplexers are used as test selectors to select the ICs either in a normal mode or a test mode. Analysis results show that the stuck-at-faults at the combinational logic IC of xx855 can be detected by the test circuit.

Keywords: *Stuck-At-Faults, Combinational Logic ICs, Built-In Self Test Circuit, Linear Feedback Shift Register, Multiplexers*

1. Introduction

Nowadays, almost all of integrated circuits (ICs) are complementary metal oxide semiconductors (CMOS) [1], [2],. They have advantages than before, i.e. lower power consumption and higher speed responses [3].

Many kinds of CMOS combinational logic ICs are made for specific functions [4],[5]. However, stuck-at-faults may occur at input and output gates inside the combinational logic ICs [6]. The faults may be caused by an imperfect manufacturing process [7]. Furthermore, the faults may generate the functions of the ICs become errors [8]. Thus, they should be detected earlier before delivering the ICs to customers.

There are two types of the faults, namely stuck-at-1 and stuck-at-0 [9]. Logic values of the gate become H values caused by the stuck-at-1. On the other hand, the stuck-at-0 may cause the logic values of the gate become L values.

A built-in self test (BIST) circuit was proposed to detect the faults [10]. However, only single stuck-at-fault may be detected by it. So, it is difficult to detect the faults in a combinational logic IC since many input and output gates the IC.

In this paper, a BIST circuit is proposed to detect stuck-at faults namely stuck-at-1 as well as stuck-at-0 occurring at input and output gates of a combinational logic IC. An analysis circuit design and analysis results are denoted in this paper.

2. Research Method

A built-in self test (BIST) circuit is proposed to detect stuck-at-faults at input and output gates inside CMOS combinational logic ICs. The test circuit is shown in Figure 1. The test circuit consist of a linear feedback shift register (LFSR) and multiplexers, M_1 to M_n.

The LFSR is made by D-flip flops and an XOR gate. Each output of the D-flip flops is connected to one of inputs of each the multiplexer. The LFSR is used to generate test vectors. Numbers of the generated test vectors based on numbers of digital inputs, Di_1 to Di_n. TCK and RST are a test clock signal and a reset signal, respectively.

The multiplexers are used to select the BIST either in a normal mode or a test mode. When an H logic value is provided to a test mode select (TMS), the BIST is in the normal mode. Logic values of the digital inputs, will be propagated directly to a combinational logic gate in which as a circuit under test (CUT). However, the BIST is in the test mode by providing an L logic value to the TMS.

Seminar Nasional Teknologi dan Rekayasa (SENTRA) 2018
ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

Thus, output logic values of the LFSR will be propagated to the CUT regardless logic values of the digital inputs.

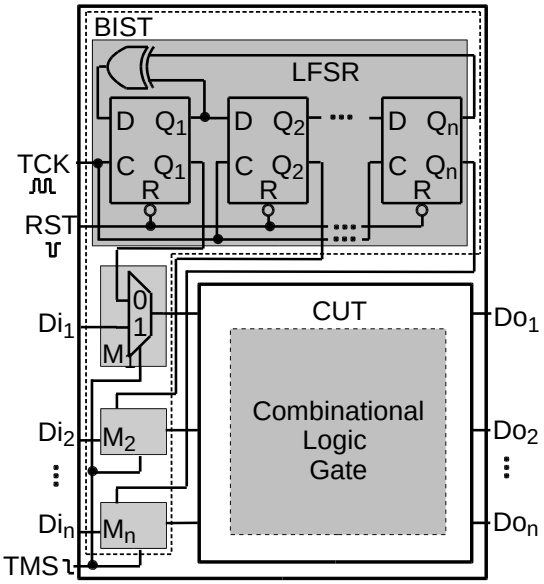

Figure 1 BIST

Stuck-at-faults may occur at input and output gates inside the combinational logic gate as the CUT. There are two types of the faults, i.e. stuck-at-1 and stuck-at-0. For example, when a s-a-0 occurs at node *i* of a combinational logic gate as a CUT in Figure 2, a digital output of Do_2 become an *L* logic value regardless logic values of nodes *d* and *f*.

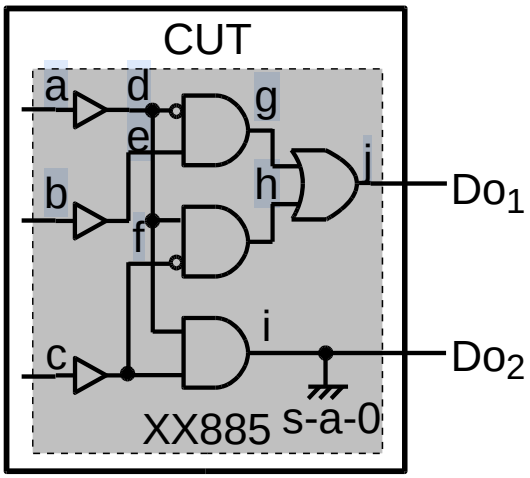

Figure 2 Combinational logic gate

3. Results and Discussion

In order to evaluate testability of a BIST circuit for detecting stuck-at-faults in a combinational logic gate, an analysis circuit is proposed by using XX855 from Nexperia Semiconductor Co. Ltd. as a CUT. The analysis circuit is shown in Figure 3. The used faults are stuck-at-1 and stuck-at-0 inserting to input and output gates of the CUT.

Analysis results are summarized in Table 1. The results are defect-free and defective circuit. The defect-free circuit is derived from a normal mode by providing an H logic value to a TMS. On the other hand, an L logic value is provided to the TMS for deriving the defective results in a test mode. The results show that the faults may be detected by the BIST circuit. The detected faults are denoted by shading in Table 1.

Seminar Nasional Teknologi dan Rekayasa (SENTRA) 2018
ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

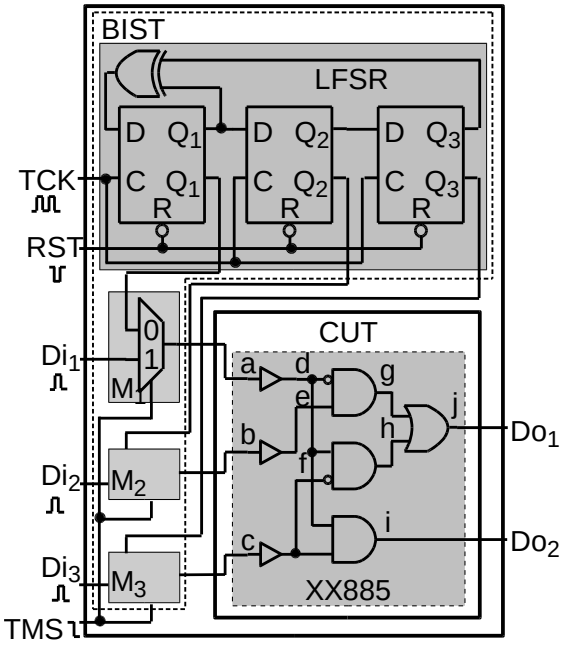

Figure 2 Analysis circuit

Table 1 Analysis results

Condition	o	LFSR 00	01	10	11	00	01	10	11
Defect-free	o_1								
	o_2								
a,d (s-a-1)	o_1	■			■				
	o_2		■		■				
a,d (s-a-0)	o_1				■	■			■
	o_2				■		■		■
b,e (s-a-1)	o_1	■	■						
	o_2								
b,e (s-a-0)	o_1			■	■				
	o_2								
c,f (s-a-1)	o_1					■		■	
	o_2					■		■	
c,f (s-a-0)	o_1						■		■
	o_2						■		■
g,h (s-a-1)	o_1		■				■		■
	o_2								
g (s-a-0)	o_1			■	■				
	o_2								
h (s-a-0)	o_1					■		■	
	o_2								
i (s-a-1)	o_1								
	o_2	■	■	■	■	■		■	
i (s-a-0)	o_1								
	o_2						■		■

4. Conclusion

Stuck-at-faults occurring at input an output gates inside a combinational logic IC may be detected by a BIST circuit. The faults are stuck-at-0 and stuck-at-1. Analysis results show that the faults can be detected.

Seminar Nasional Teknologi dan Rekayasa (SENTRA) 2018
ISSN (Cetak) 2527-6042
eISSN (Online) 2527-6050

References

[1] Neil HEW, David MH. A Circuit and Systems Perspective. Fourth Edition. Addison Wesley. 2011.
[2] Jan MR, Anantha C, Borivoje N. Digital Integrated Circuits A Design Perspective. Pearson Education. 2002.
[3] Richard CJ, Travis NB. Microelectronic Circuit Design. Fourth Edition. McGraw Hill Company. 2011.
[4] Steve K, Yusuf L. CMOS Digital Integrated Circuits Analysis and Design. Second Edition. McGraw Hill Company. 2003.
[5] Thomas LF. Digital Fundamentals A System Approach. Pearson Education. 2014.
[6] Michael LB, Vishwani DA. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits. Kluwer Academic Publishers. 2002.
[7] Baker RJ. CMOS Circuit Design, Layout, and Simulation. Jhon Wiley & Son Inc. 2010.
[8] Edward JM, Chao-Wen T. *Stuck Fault Tests vs Actual Defects*. Proceeding of IEEE International Test Conference (ITC). Pp. 336-342, 2000.
[9] Laung-Terng W, Cheng-Weng W, Xiaoqing W. VLSI Test Principles and Architectures. Morgan Kaufman Publihers. 2006.
[10] LLavius O, Mircea V. *Evaluating the Self Testing Property of AES Finite Field Inversion Unit*. Proceeding of IEEE European Test Symposium (ETS), Pp. 1-2, 2015.