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OPEN DEFECT DETECTIONS OF CMOS ICS BY USING I_{DDQ} TESTING

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Abstract

An I_{DDQ} testing is proposed to detect an open defect at an input gate in a CMOS IC. The testing is based on measuring a quiescent supply current I_{DDQ} on the IC. When the open defect occurs at the input gate, the large I_{DDQ} will flow to the IC regardless test input vectors which generate to it. On the other hand, in the defect-free IC, the large I_{DDQ} does not flow to the IC. The testing is implemented in the CMOS IC designed by a Spice net list library of NXP Co. Ltd and is examined using a Spice simulation. Simulation results show that the open defect can be detected by the I_{DDQ} testing.

Keywords: *I_{DDQ} testing, open defect, input gate, CMOS IC*

1. Introduction

Recently, the density and the complexity of CMOS (complementary metal oxide semiconductor) ICs (integrated circuits) increase significantly [1]. It makes a challenge to test the ICs before shipping to customers, where open and short defects could occur at its input gates.

The short defects are bridging between two or more metal lines in the ICs. Most the shorts are caused by extra conducting materials [2]. I_{DDQ} testing technique has been proposed to detect the short defects [3]. The defects can be detected by measuring a large quiescent supply current I_{DDQ} flows in the ICs.

The open defects are opens at metal lines. They are caused by the increasing number contacts and vias [4]. The defects can be detected by the I_{DDQ} testing [5]. However, test input vectors should be determined earlier to detect the defects.

In this paper, an I_{DDQ} testing is proposed to detect an open defect at an input gate in a CMOS IC regardless generated test input vectors. Analysis results were denoted to evaluate the feasibility of the testing in detecting the defect.

2. IDDQ Testing

A testable DUT (device under test) IC is made of the proposed I_{DDQ} testing shown in Fig. 1. As shown in Fig. 1, the IC is made of input protection circuits, inverters, a logic core, and output protection circuits. A targeted open defect is denoted by "a".

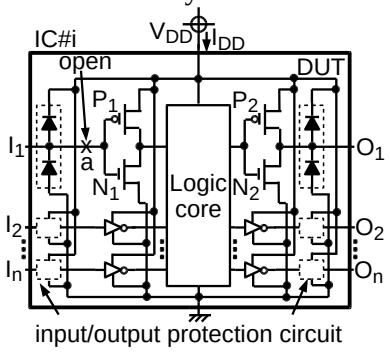

Figure 1 DUT

Electrical characteristics of the inverter gate which is between the input protection circuit and the logic core are shown in Fig. 2. As shown in Fig. 2(b), when an input voltage of the gate *Vi* is a *H* or a *L* level, supply current i_{DD} of almost zero will flow into the gate. On the other hand, if *Vi* is in a

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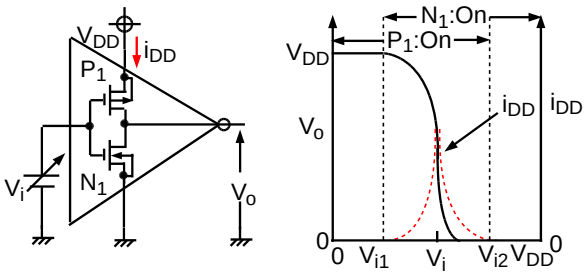
range specified by Eq. (1), large i_{DD} will flow, since both a pMOS P_1 and an nMOS N_1 in the gate turn on.

$$Vi_1 \leq Vi \leq Vi_2 \quad (1)$$



(a) Measurement circuit (b) DC characteristics

Figure 2 DC characteristics of inverter gate

When an open defect occurs at *a*, a large quiescent supply current I_{DDQ} flows to the IC, regardless either a *H* or a *L* level is provided to an input of the IC I_1, since the input voltage of the inverter is the range specified Eq. (1). However the I_{DDQ} is almost zero flows in the defect-free IC, when the input voltage of the inverter is either the *H* or the *L* level.

3. Result and Discussion

A simulation circuit is made to evaluate the feasibility of the proposed I_{DDQ} testing as shown in Fig. 3. The circuit is made of two ICs, *IC#i*-1 and *IC#i*. Each of the ICs is designed using a Spice netlist library distributed by NXP. CO. Ltd. A targeted open defect is denoted by "*a*" in the DUT of *IC#i*.

The power supply voltage 3.3 V and a resistor 1 *T*Ω are provided to V_{DD} and *a*, respectively. The simulation results are summarized in Fig. 4. As shown in Fig. 4, when an open defect occurs at *a*, a quiescent supply current I_{DDQ} flows to the circuit.

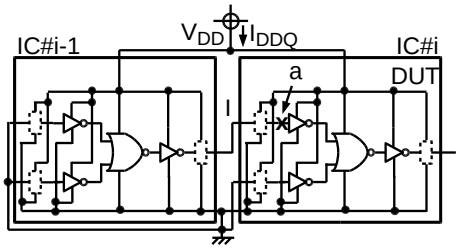


Figure 3 Simulation circuit

A simulation circuit is made to evaluate the feasibility of the proposed I_{DDQ} testing as shown in Fig. 3. The circuit is made of two ICs, *IC#i*-1 and *IC#i*. Each of the ICs is designed using a Spice netlist library distributed by NXP. CO. Ltd. A targeted open defect is denoted by "*a*" in the DUT of *IC#i*.

4. Conclusion

An I_{DDQ} testing was proposed to detect an open defect in a CMOS IC. The feasibility of the testing was evaluated by a Spice simulation. The simulation results show that the open defect can be detected by the large I_{DDQ} flows to the IC. It remains a future work, the open defect should be located by the testing.

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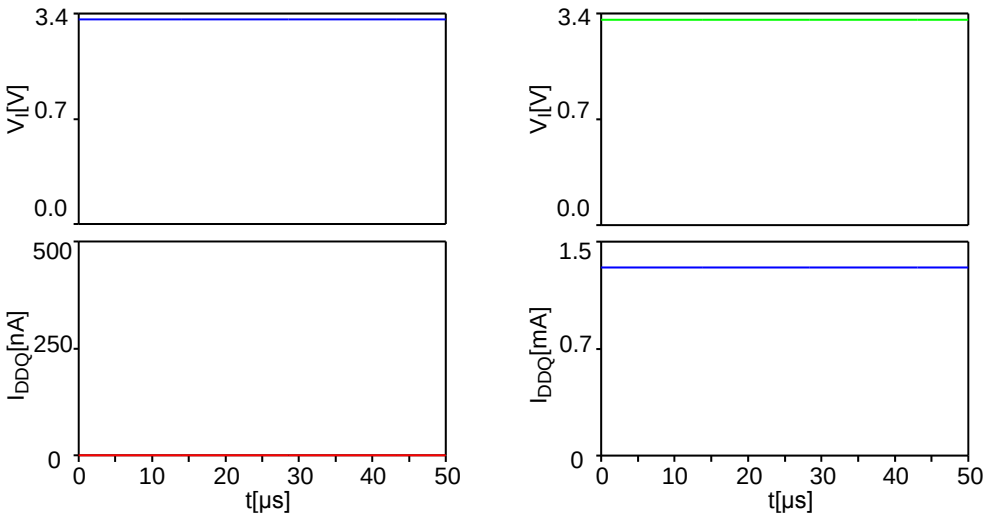

(a) Defect-free IC (b) Defective one

Figure 4 Simulation results

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